100 W single-stage CrCM PFC Flyback converter using the IRS2982S and IR1161L

Application note

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About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to using the DEMO_100W_24VDC_FB single-stage PFC Flyback power supply evaluation board based on the IRS2982S and IR1161L controllers. It describes the operation and covers technical aspects essential to the design process, including calculation of external component values, MOSFET selection and PCB layout optimization, as well as additional protection circuitry that may be added if needed. Test results and waveforms are also included.

Intended audience

Power supply design engineers, applications engineers, students.

Table of contents

1 Introduction

The IRS2982S is a versatile SMPS controller IC primarily intended for power supply and LED drivers in the 5 to 100 W power range suitable for buck, buck-boost and Flyback converters operating in Critical Conduction Mode (CrCM) and Discontinuous Conduction Mode (DCM) at light loads. Flyback converters will be covered in this application note, focusing on an isolated voltage-regulated design with Power Factor Correction (PFC). All of the control and protection required for the converter is integrated in the IRS2982S as well as a HV start-up cell to enable rapid start-up at switch-on over a wide line input voltage range. The IRS2982S is also able to provide PFC in a single-stage Flyback converter able to meet class D line current harmonic limits of the EN 61000-3-2 standard.

A 100 W isolated constant voltage-regulated PFC Flyback evaluation board based on the IRS2982S controller is described in detail in this application note and detailed test results are presented.

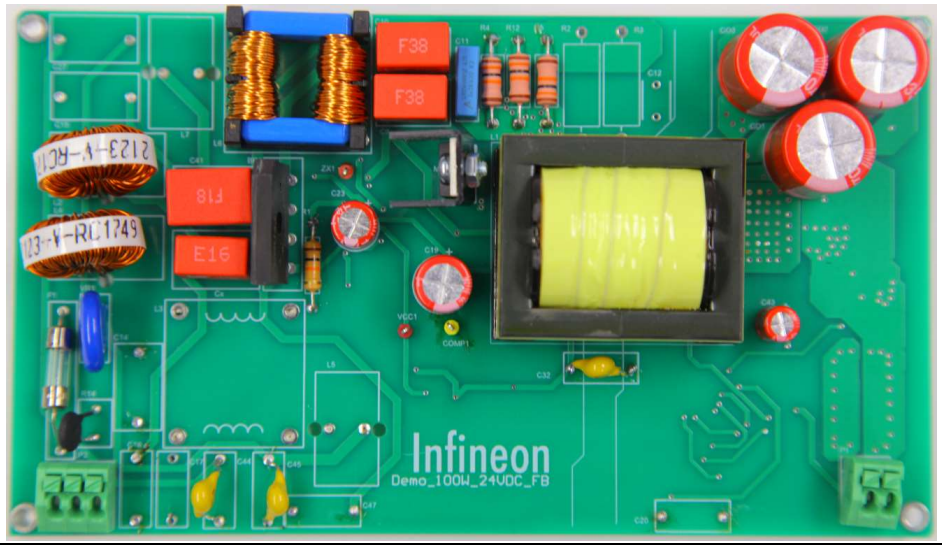


Figure 1 **DEMO_100W_24VDC_FB single-stage PFC Flyback converter demo board (top view)**

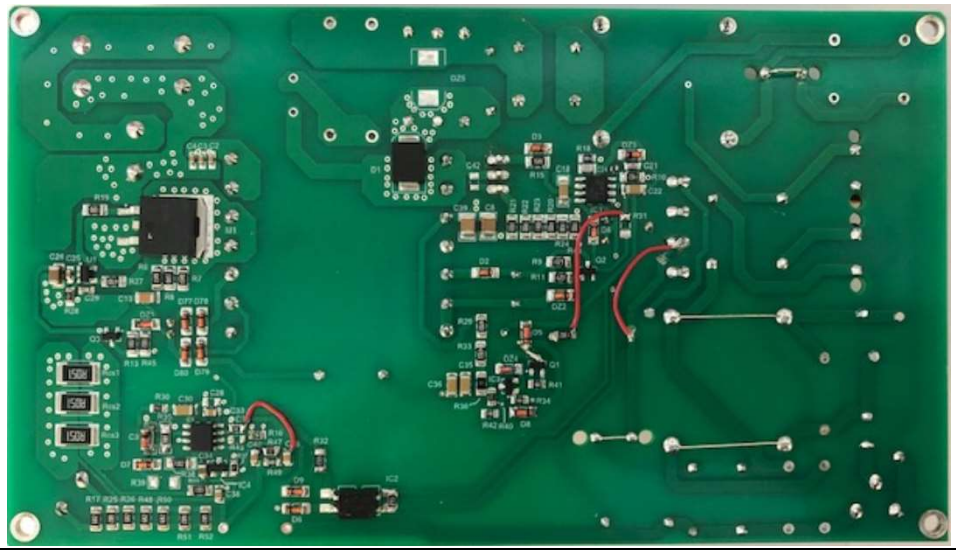


Figure 2 **DEMO_100W_24VDC_FB single-stage PFC Flyback converter demo board (bottom view)**

2 Evaluation board specifications

Input and output at normal operation

- AC input voltage 90 to 265 V_{RMS} (55 to 65 Hz)
- Output voltage 24 V
- Output current 4.2 A
- Maximum output continuous power 100 W
- PF greater than 0.9 at maximum load, 90 V AC to 265 V AC input voltage
- Total Harmonic Distortion (iTHD) less than 20 percent at maximum load, to 265 V_{RMS} input voltage
- Start-up time to reach the secondary nominal output voltage during full-load condition at 120 and 230 V_{RMS} input voltage less than 2 s

Protection features

- Output Over-Voltage Protection (OVP) at V_{OUT} less than or equal to 25 V
- Over-Current Protection (OCP) at 5.5 A
- Short-Circuit Protection (SCP)
- Brown-out protection, shut-down at 60 to 65 V_{RMS}, start-up at 85 to 90 V_{RMS} AC input voltages

No-load operation

- Burst mode during no-load condition
- Maximum power loss during no-load condition is 1.6 W at 120 and 230 V_{RMS} input voltage

Maximum component temperature

In an ambient temperature of 30°C, the maximum allowed component temperatures are as follows:

- Resistors less than 100°C
- Ceramic capacitors, film capacitors and electrolytic capacitors less than 100°C
- Flyback transformer less than 100°C
- MOSFET transistors and diodes less than 100°C
- ICs less than 100°C

Dimensions of evaluation board

Maximum width 6.5 inches (165.3 mm), maximum length 3.72 inches (94.5 mm)

WARNING!

The board should be tested only by qualified engineers and technicians.

3 Schematics

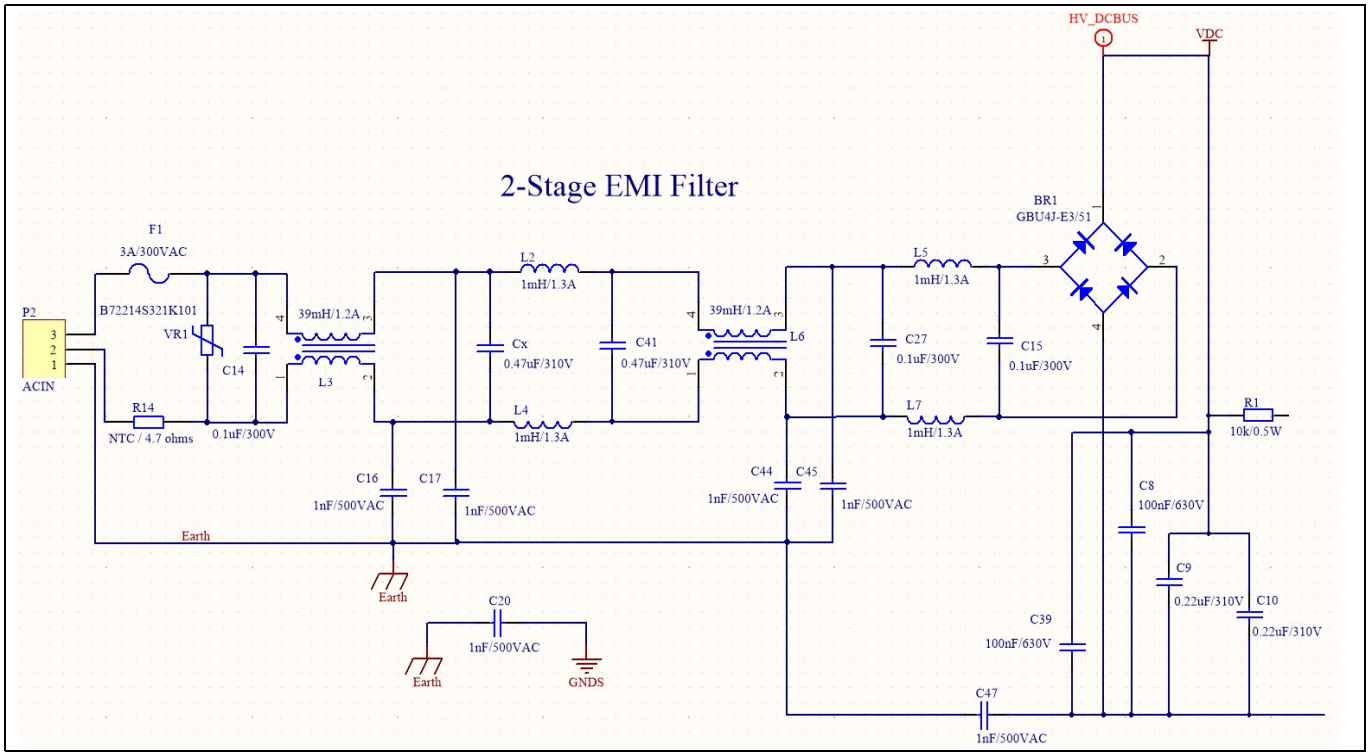


Figure 3 Single-stage PFC Flyback converter (input filter)

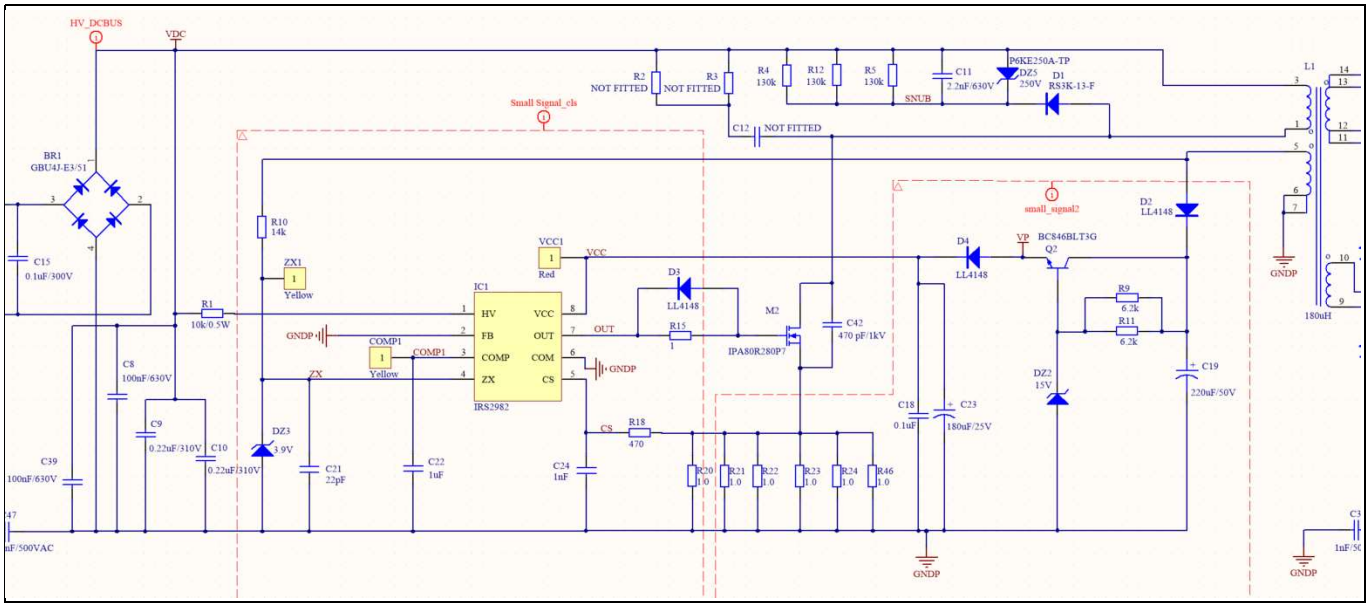


Figure 4 Single-stage PFC Flyback converter (primary DC side)

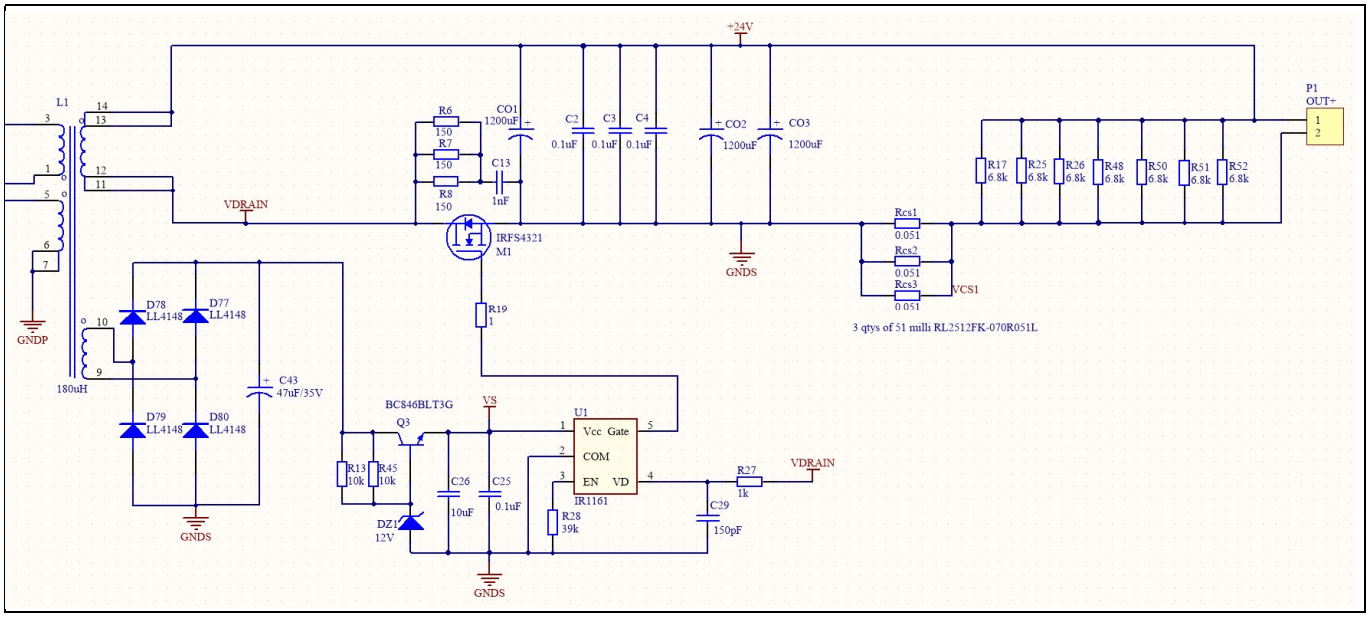


Figure 5 Secondary side of PFC Flyback

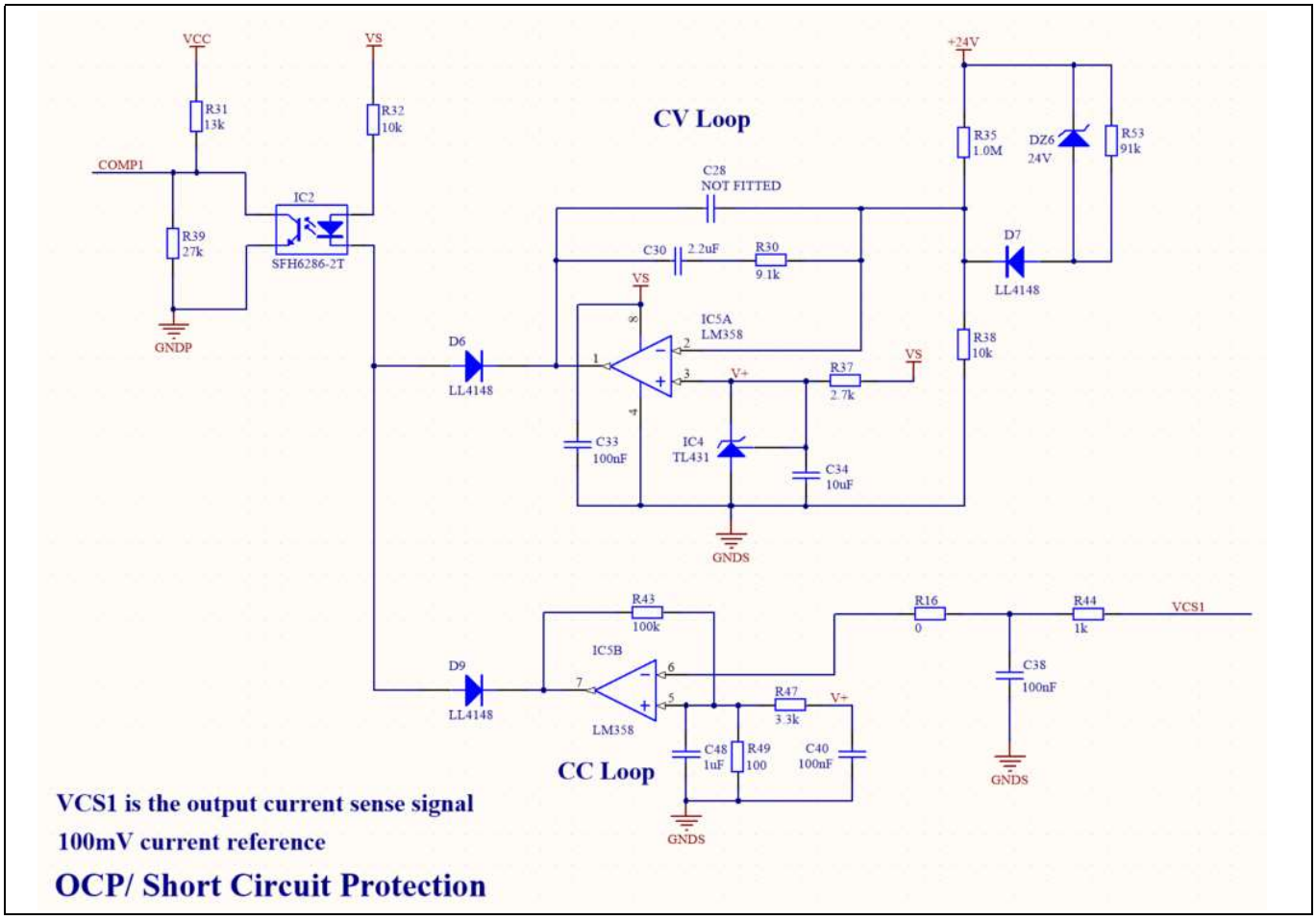


Figure 6 Voltage feedback amplifier and over-current protection

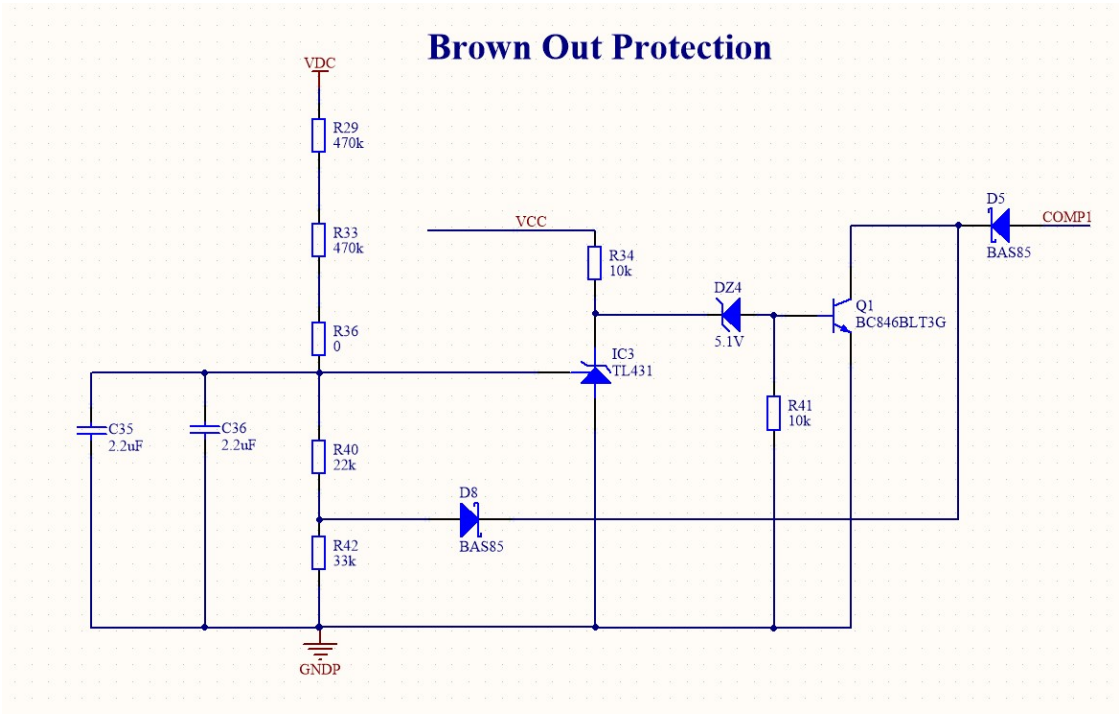


Figure 7 Brown-out protection

4 IRS2982S functional overview

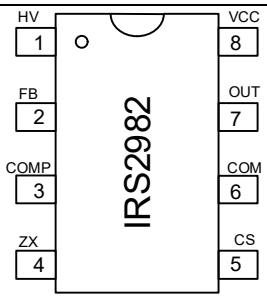
The IRS2982S is comprised of the following functional blocks:

1. *HV start-up cell*
   The IC internal functional blocks remain disabled in low-power mode until V_{CC} first rises above the V_{CCUV+} Under Voltage Lockout (UVLO) threshold, continuing to operate while V_{CC} remains above V_{CCUV-}. V_{CC} is initially supplied through the integrated HV start-up cell, which supplies a controlled current from the HV input provided a voltage greater than V_{HVSMIN} is present. The current supplied is limited to I_{HV_CHARGE}, reducing to less than I_{HVS_OFF} when V_{CC} reaches the cut-off threshold V_{HVS_OFF1}. The HV start-up cell switches over from start-up mode to support mode after the feedback input at FB has exceeded V_{REG} for the first time. In this mode the cut-off threshold becomes V_{HVS_OFF2}. During steady-state operation under all line-load conditions V_{CC} is supplied through an auxiliary winding on the Flyback transformer with V_{CC} high enough so that the HV start-up cell does not supply current. If the auxiliary supply were unable to maintain V_{CC}, the HV start-up cell operating in support mode would supply current to assist.

2. *PWM controller*
   The SMPS control section operates in voltage mode where the gate drive output on-time is proportional to the error amplifier output voltage appearing at the compensation output COMP. An external capacitor C_{COMP} (shown in Figure 8) connected to 0 V (ground) acts with the trans-conductance characteristic of the error amplifier to provide loop compensation and stability. Minimum on-time is reached when V_{COMP} falls to $V_{COMPOFF}$, below which the gate drive is disabled. Under very light-load conditions V_{COMP} transitions above and below $V_{COMPOFF}$ to produce burst-mode operation. Off-time is determined by the demagnetization signal received at the ZX input, which is derived from the auxiliary transformer winding that supplies V_{CC} through a resistor divider. Internal logic limits the minimum off-time to t_{OFFMIN}, therefore the system transitions from CrCM to Discontinuous Conduction Mode (DCM) at light loads. If the ZX input signal fails to provide triggering the next cycle will start automatically after a restart period of t_{WD}.

3. *Protection*
   The IRS2982S includes cycle-by-cycle primary OCP, which causes the gate drive to switch off if the voltage detected at the CS exceeds the threshold V_{CSTH}. This prevents the possibility of transformer saturation at low-line under heavy load, but does not protect against output over-load or short-circuit.

OVP is also provided through the ZX input, which provides a voltage proportional to the output voltage. This disables the gate-drive output and pulls the COMP voltage below the $V_{COMPOFF}$ threshold. The error amplifier then starts to charge C_{COMP} until the gate drive starts up again at minimum on-time. Under an open-circuit output condition the OVP causes the converter to operate in burst mode, preventing the output voltage from rising too high. The IRS2982S uses an SO-8 package, as shown below:



Pin	Name	Description
1	***HV***	HV start-up input
2	***FB***	Feedback input
3	***COMP***	Compensation and averaging capacitor input
4	***ZC***	ZC and OV detection input
5	***CS***	CS input
6	***COM***	IC power and signal ground
7	***OUT***	Gate-driver output
8	***V_{cc}***	Logic and low-side gate-driver supply

Figure 8 IRS2982S pin assignments

5 Flyback converter

5.1 Flyback converter types

There are several configurations of Flyback converter that may be used with the IRS2982S depending on the application. These can be classified according to isolation and regulation requirements as follows:

1. Isolated or non-isolated
2. Current or voltage regulation
   In the case of voltage regulation current limiting is needed for protection against over-load or short-circuit, and in the case of current regulation OVP is necessary for an open circuit.

The IRS2982S can operate in any of the four combinations of (1) and (2). Extremely accurate current or voltage regulation is achieved in non-isolated converters since direct feedback to the FB input is possible. Isolation is however required in the majority of Flyback converters, therefore for isolated constant voltage and/or regulation as used in this design, an opto-isolator is needed. Primary side regulation from the auxiliary transformer winding as shown in the figure below is unable to produce sufficient accuracy due to the leakage inductance, which causes ringing oscillations that result in poor tracking between the rectified DC output voltage and the rectified auxiliary winding voltage. . From reference [4], it can be seen that very low leakage inductance is needed for primary side regulation to achieve reasonably accuracy and it would probably be impossible to meet isolation requirements in such a transformer design

The basic circuit below shows the main elements of the IRS2982S-based PFC Flyback converter. This single stage converter is able to provide a regulated output voltage over a wide range of line and load with sufficient accuracy for the many applications.

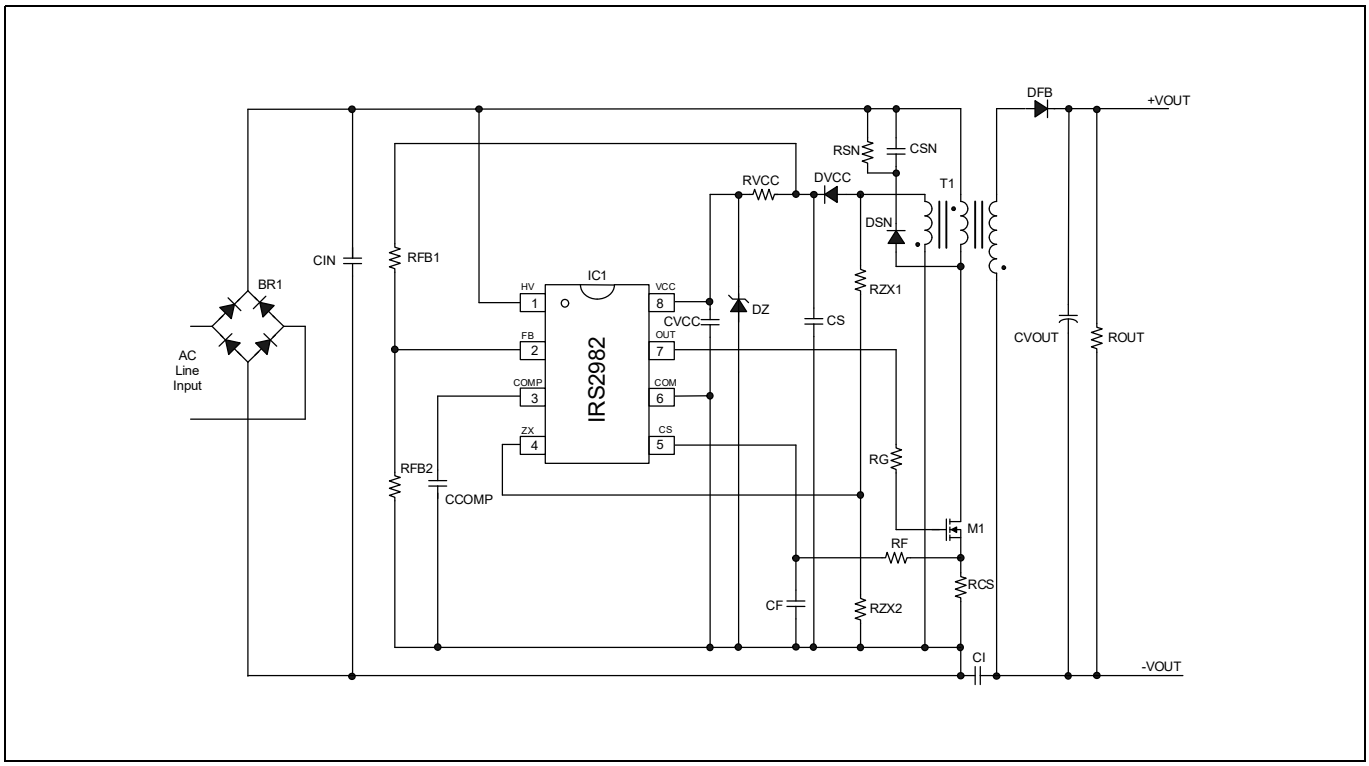


Figure 9 Isolated voltage primary side regulated Flyback converter based on the IRS2982S

6 IR1161L functional overview

The IR1161L smart secondary-side controller drives an N-channel power MOSFET used as a synchronous rectifier (SR) in isolated Flyback converters operating in DCM or quasi resonant (QR) mode, also known as CrCM, transition or Boundary Mode (BCM). A pair of IR1161L controllers and MOSFETs may be also be used as a dual SR in resonant half-bridge converters.

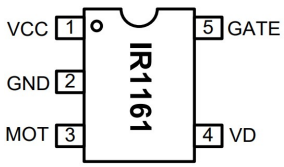
The IR1161L precisely controls switching on and off of the synchronous MOSFET thereby bypassing its body diode during the secondary conduction phase and emulating the rectifying action of a diode rectifier while eliminating the majority of conduction losses. The MOSFET drain to source voltage is sensed at millivolt levels to determine the polarity of the drain current switching the gate on and off in close proximity to the zero current transition. The HV input structure allows the IR1161L to withstand up to 200 V from direct connection to the drain.

Internal blanking, reverse current protection circuit and double-pulse suppression provide safe and reliable operation. The IR1161L-based smart SR offers significant efficiency improvement in DCM Flyback converters over the full load range so that replacing a Schottky diode output rectifier with the IR1161L and a correctly selected high-performance MOSFET provides significantly lower power dissipation. PCB space savings due to the IR1161L's small SOT23-5 package are further aided by reduced MOSFET heat dissipation.

The IR1161L is able to operate from a wide V_{CC} supply voltage ranging from 4.75 to 20 V, making it possible to supply it from the output in a 5 V system and eliminating the need for an auxiliary winding. A logic-level MOSFET is required for low output voltage applications.

A built-in arming and triggering mechanism is included to allow correct switching on and off of the SR MOSFET under all system conditions, making it superior to a basic self-driven SR scheme or earlier generations of SR controller.

IR1161L is available in a 5-pin SOT-23 package. The pin-out is shown below:



Pin	Name	Description
1	***VCC***	Supply voltage
2	***GND***	Ground
3	***MOT***	Minimum on-time program input
4	***VD***	FET drain sensing
5	***GATE***	Gate-drive output

Figure 10 IR1161L pin assignments

Referring to the diagram below, T1 is the conduction phase of the primary switch during which energy is being stored in the Flyback transformer. The T2 phase begins when the primary switch is turned off and the energy stored in the magnetic field starts to be delivered to load through the output rectifier circuit. At this point the conduction phase of the SR MOSFET is initiated, and current starts flowing through the body diode, generating a negative V_{DS} voltage. The body diode has a much higher voltage drop than the turn-on threshold V_{TH1}, causing the IR1161L to drive the gate of the SR MOSFET on to bypass it. When the MOSFET is turned on the instantaneous sensed voltage reduces to $I \cdot R_{DS(on)}$. This voltage level, being much lower than the body diode

forward voltage drop, is sensitive to parasitic ringing generated by the transformer leakage inductance and MOSFET output capacitance. To avoid mis-triggering and resulting premature gate turn-off, a blanking period (MOT) is used that disables V_{TH1} triggering for a minimum period of time set by an external resistor.

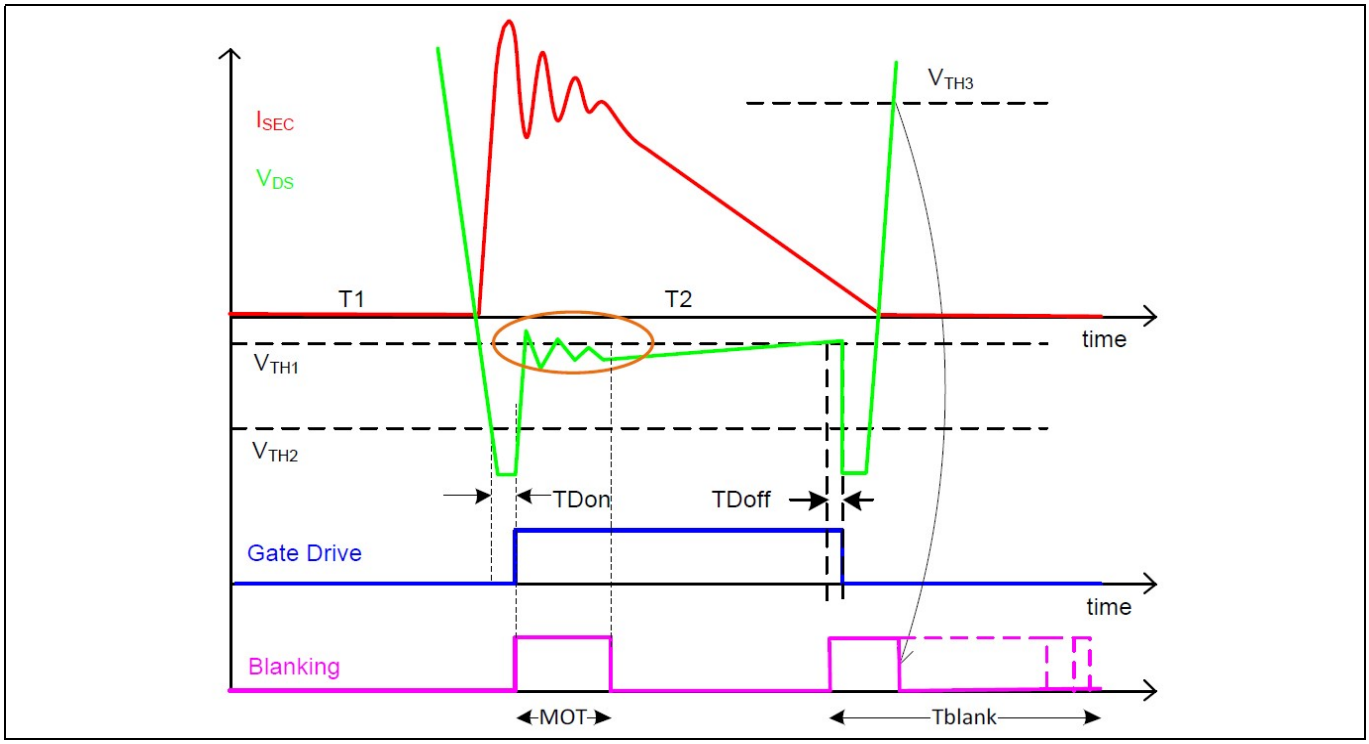


Figure 11 Secondary SR waveforms of DCM/CrCM Flyback

At the end of each switching cycle the secondary current reduces to zero and the V_{DS} voltage crosses the turn-off threshold V_{TH1}. The IR1161L then turns the gate off and current will again start flowing through the body diode, causing the V_{DS} voltage to make a sharp negative transition. Depending on the amount of residual current, V_{DS} may once again exceed the turn-on threshold V_{TH2}. For this reason re-triggering is disabled after the gate drive has been switched off until the controller has re-armed. The re-arming sequence requires V_{DS} to cross the V_{TH3} threshold and remain above it for a period denoted as t_{BRST}. If this does not occur, the gate drive will remain low for a period of t_{BLANK}, after which time re-arming will occur automatically.

To achieve high system efficiency and low standby loss at the same time, the IR1161L incorporates a programmable minimum on-time. This feature offers flexibility in various applications at different switching frequencies. The MOT function determines the shut-down point at light load. During normal operation, the designer sets the minimum on-time to be shorter than the secondary conduction period. At progressively lighter loads, the conduction period reduces until it eventually becomes shorter than the MOT. If the IR1161L detects no voltage drop signifying no SR drain current the MOT protection function causes the gate drive to remain off for the next cycle. MOT protection operates whether or not the SR gate drive is active or whether conduction is through the body diode. In this way the IR1161L does not drive the gate at light loads and therefore consumes minimal power, improving system efficiency.

7 Design calculations

The principle of operation for the single-stage PFC Flyback converter is that it uses an unsmoothed DC bus voltage with only a small high-frequency capacitor to maintain a full wave-rectified voltage profile. The converter operates in CrCM under normal operating conditions with the on-time remaining effectively constant over the period of the AC-line cycle. This results in an approximately sinusoidal average input current with minimal phase shift and distortion. The output current or voltage is regulated by controlling the on-time using a FB loop that responds to line and load changes.

One of the principal advantages of operating a power supply in CrCM is that the power stage appears as a first-order system and is therefore easier to stabilize. Please see reference [5], which goes into detail about the modeling of the Flyback power stage and compensating it using type-II error amplifier compensation. The second advantage of using CrCM is that there is no reverse recovery (t_{rr}) loss in the output diode since the primary switch is turned on when the output diode current reaches zero. This being the case, the selection of the output diode is quite straightforward, as super-fast recovery time is not required. The third advantage is that if the MOSFET is turned on in the drain voltage valley the capacitive switching loss due to C_{oss} is reduced significantly [7]. On the other hand the drawbacks of CrCM are that the operating frequency varies in relation to the input and output conditions. The frequency increases during light-load conditions, which can increase switching losses. In order to limit switching frequency the IRS2982 incorporates a minimum off-time of 3 µs, which limits the maximum switching frequency, thereby limiting the switching losses. At full load the frequency is at minimum. During this period conduction losses dominate over switching losses. CrCM operation involves high peak and RMS currents compared to CCM operation. During low-line and full-load conditions the switching frequency can decrease enough to enter the audible range if the primary inductance value is too high.

The advantages such as ease of design, simple compensation and low switching losses increase the overall efficiency of the converter. The advantages of CrCM operation outweigh the disadavantages.

The evaluation board described here is designed to provide a constant output voltage of +24 V, as shown in Figure 3. It consists of a Flyback converter designed for PFC with low AC-line iTHD. The MOSFET used is an IPP80R360P7 800 V rated CoolMOS™ device with 360 mΩ on-resistance and 30 nC gate charge in a TO-220 package. This device is able to withstand HV ringing at switch-off with minimal added snubber components and has low conduction and switching losses as well low gate-drive current. The CoolMOS™ P7 series offers high performance though optimizing key parameters (C_{oss}, E_{oss}, Q_g, C_{iss} and $V_{GS(th)}$, etc.), integrating a Zener diode for ESD protection and other measures. This product family fully addresses design needs, ease of use and price/performance ratio, delivering best-in-class performance. The 700 V and 800 V CoolMOS™ P7 series have been designed for Flyback converters and could also be used in PFC topologies.

A synchronous MOSFET is used on the secondary side for achieving lower loss and high efficiency compared to using a rectifiying diode. The synchronous MOSFET is a IPB073N15N5. This is a 150 V D^2PAK device with 7.3 mΩ on-resistance and 49 nC gate charge being driven by the IR1161L. If a diode is used on the secondary side instead of a MOSFET the losses would be quite high at full load current of 4.2A and it would be necessary to use a heatsink.

The parameters of the primary and secondary MOSFETs contribute to the overall high efficiency of the converter. The design of the transformer is critical. Reducing the core losses and the winding losses play an important role in the converter efficiency. The Flyback transformer (more accurately described as a coupled inductor) consists of four windings; the primary for energy storage during the on-time, the secondary for energy transfer to the output during the off-time and the auxiliary, which supplies V_{CC} to the IRS2982 and provides the required de-magnetization and voltage FB signals. The second auxiliary winding is on the secondary side to supply the IR1161L and also plays an important role in feedback loop, which will be described later.

The IRS2982S (IC1) V_{CC} supply is derived from the transformer auxiliary winding through D4 initially charging C19 and then C23 through an NPN transistor, parallel combination of R9, R19 and a series diode D4 with DZ2 to clamp the voltage to protect IC1 from over-voltage. The FB pin of the IC is grounded since secondary-side regulation is being used to provide a stable 24 V output. The zero crossing of the transformer secondary current is detected using an auxiliary winding on the primary side. At the input AC line zero crossing the auxiliary voltage is not high enough to trigger the zero crossing (ZX) so the ZX voltage may remain below 1.54 V, which results in no gate pulses. This causes little reduction in the THD. On this demo board a Zener diode of 3.9 V is used at the ZX pin to allow continuous switching through the line zero crossing by eliminating the functionality of OVP using this ZX pin. This is not a concern on this demo board since secondary-side voltage regulation also takes care of the over-voltage. Under a no-load condition the voltage remains constant at around 24 V.

Switching-cycle peak current limiting is set by parallel shunt resistors R20 to R24, which give a combined resistance of 200 mΩ, setting the peak current to 6 A according to the threshold V_{CSTH} of 1.2 V. This limits the inrush current during start-up and also protects against damage under over-load or short-circuit conditions. At the input AC-line after the fuse an NTC thermistor of 5 Ω is also used to reduce the inrush current. The NTC resistor starts with a higher resistance when cold and reduces its resistance when the temperature of the NTC increases. The evaluation board is not designed to withstand a sustained output over-load or short-circuit.

Table 1 PFC Flyback converter specifications

AC input voltage	90 to 265 V_{RMS}
Input line frequency	47 to 63 Hz
Nominal DC output voltage	24 V
Maximum output power	100 W
Power factor	0.99 at 120 V_{RMS}/100 W 0.99 at 230 V_{RMS}/100 W
Start-up time	1.5 s
Minimum switching frequency	60 kHz
OVP	24.5 V

The maximum peak current at low-line and full load, assuming D_{MAX} is 0.58, is calculated as:

$$L = \frac{V_{acmin}^2 \cdot \eta \cdot D_{max}^2}{2 \cdot P_{out} \cdot f_{min}} \quad [\text{H}] \qquad [1]$$

$$\frac{85^2 \cdot 0.9 \cdot 0.58^2}{2 \cdot 100.8 \cdot 60000} = 180.8\mu\text{H}$$

The peak inductor current is then calculated from:

$$I_{pk} = \frac{\sqrt{2} \cdot V_{acmin} \cdot D_{max}}{L_p \cdot f_{min}} \quad [\text{A}] \qquad [2]$$

$$\frac{\sqrt{2} \cdot 85 \cdot 0.58}{181 \cdot 60000} = 6.426\ A$$

The CS resistor (R_{CS}) is then calculated:

$$R_{CS} = \frac{V_{CS(th)}}{I_{Trip}} \quad [\Omega] \quad [3]$$

$$I_{Trip} = 1.1 \cdot I_{PK} = 7.068$$

$$R_{CS} = \frac{1.26\ \mathrm{V}}{7.068} = 0.18\ \Omega$$

In this case a parallel combination with a combined resistance of 0.2 Ω has been used.

7.1 Voltage feedback and loop compensation

The input-to-output DC transfer characteristic for the Flyback converter is given by:

$$\frac{V_{out}}{V_{in}} = \frac{N_s}{N_p} \cdot \frac{D}{1-D} \quad [4]$$

The voltage mode Flyback converter operating in DCM or CrCM/BCM has a basic error amplifier output-to-converter output voltage small-signal transfer characteristic with a single pole formed by the output capacitor and load resistance and a zero formed by the output capacitor ESR:

$$F(s) = \frac{\mathrm{V_{OUT}(s)}}{\mathrm{V_{COMP}(s)}} \approx \frac{V_{OUT}}{V_{COMP}} \cdot \frac{1+\frac{s}{\omega_{z0}}}{1+\frac{s}{\omega_{po}}} \quad [5]$$

Where,

$$\omega_{po} = \frac{2}{R_{LOAD} \cdot C_{OUT}}\ ,\ R_{LOAD} = \frac{V_{OUT}}{I_{OUT}}\ \text{and}\ \omega_{zo} = \frac{1}{R_{ESR} \cdot C_{OUT}}$$

The ESR zero occurs at a relatively high frequency and does not come into play in PFC Flyback converters since these have a much slower loop speed than converters operating from DC, which are required to compensate rapidly for step changes in line or load.

The plant transfer function may therefore be simplified to:

$$F(s) = \frac{\mathrm{V_{OUT}(s)}}{\mathrm{V_{COMP}(s)}} \approx \frac{V_{OUT}}{V_{COMP}} \cdot \frac{1}{1+\frac{s}{\omega_{po}}} = \frac{V_{OUT}}{V_{COMP}} \cdot \frac{1}{1+\left(\frac{s \cdot R_{LOAD} \cdot C_{OUT}}{2}\right)} \quad [6]$$

While the pole can be easily calculated at each specific load, the relationship between V_{OUT} and V_{COMP} is non-linear and depends on several system parameters, making it necessary to evaluate it at each operating point at which the small-signal stability analysis is to be done.

For the Flyback converter operating in DCM the plant transfer characteristic is as follows:

$$\frac{V_{OUT}(s)}{d(s)} = \frac{V_{IN(RMS)}}{\sqrt{k}} \cdot \frac{1}{1+\left(\frac{s \cdot R_{LOAD} \cdot C_{OUT}}{2}\right)} \quad [7]$$

Where,

$$k = \frac{2 \cdot L_S}{R_{LOAD} \cdot T_S} = \frac{2 \cdot \frac{N_S}{N_P} \cdot L_P}{R_{LOAD} \cdot (T_{ON}+T_{OFF})} \quad [8]$$

Duty cycle depends on the input and output voltages and the transformer turns ratio. It varies during the line cycle, so for convenience the duty-cycle operating point is evaluated at a 45-degree phase angle where the instantaneous voltage is equal to the RMS voltage:

$$D = \frac{1}{1+\left(\frac{V_{IN(RMS)}}{V_{OUT}+V_F}\right) \cdot \left(\frac{N_S}{N_P}\right)} \quad [9]$$

T_{ON} is constant and can be evaluated according to:

$$T_{ON} = \frac{L_P \cdot P_{OUT}}{\eta \cdot V_{IN(RMS)}^2 \cdot D} = \frac{L_P \cdot V_{OUT}^2}{\eta \cdot V_{IN(RMS)}^2 \cdot R_{LOAD} \cdot D} \quad [10]$$

T_{OFF} varies with the full wave-rectified bus voltage :

$$T_{OFF} = \frac{\left(\frac{N_S}{N_P}\right) \cdot V_{IN(RMS)} \cdot T_{ON}}{V_{OUT}+V_F} \quad [11]$$

From equations (4) through (10) the small-signal duty cycle to output voltage transfer function can be evaluated at the operating point. The relationship between V_{COMP} and the T_{ON} for the IRS2982 is shown below:

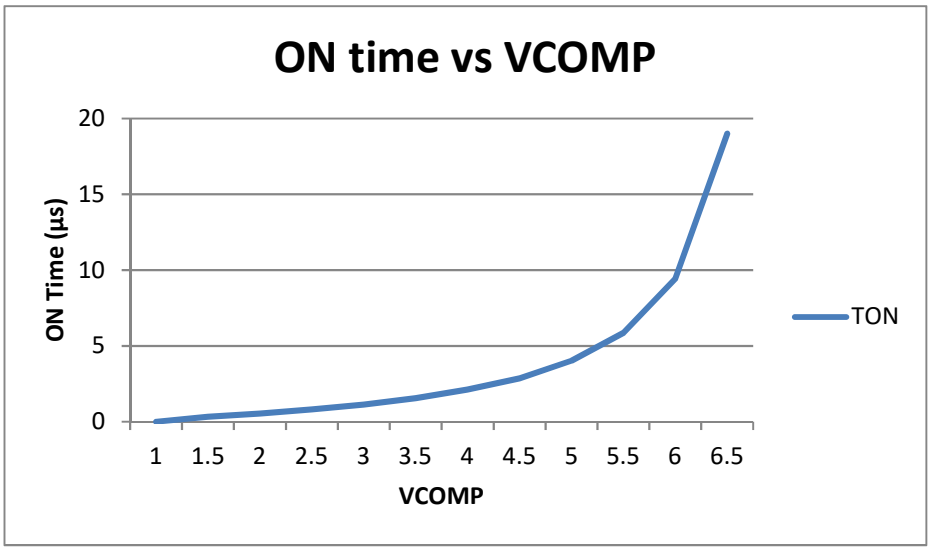


Figure 12 On-time as a function of V_{COMP}

The relationship is non-linear, defined by the polynomial equation by curve fitting:

$$T_{ON} \approx 0.0178 \cdot V_{COMP}^6 - 0.3463 \cdot V_{COMP}^5 + 2.6845 \cdot V_{COMP}^4 - 10.426 \cdot V_{COMP}^3 + 21.192 \cdot V_{COMP}^2 - 20.642 \cdot V_{COMP} + 7.5426 \quad [12]$$

The derivative of this equation provides the small-signal relationship at any operating point up to an on-time of approximately 20 µs:

$$\frac{\delta T_{ON}}{\delta V_{COMP}} \approx 0.1068 \cdot V_{COMP}^5 - 1.7315 \cdot V_{COMP}^4 + 10.738 \cdot V_{COMP}^3 - 31.278 \cdot V_{COMP}^2 + 42.384 \cdot V_{COMP} - 20.642 \quad [13]$$

Since

$$d = \frac{T_{ON}}{T_{ON}+T_{OFF}} \quad [14]$$

therefore,

$$\delta d = \frac{\delta T_{ON}}{T_{ON}+T_{OFF}} \quad [15]$$

Then

$$\frac{\delta d}{\delta V_{COMP}} \approx \frac{\left(0.1068 \cdot V_{COMP}^5 - 1.7315 \cdot V_{COMP}^4 + 10.738 \cdot V_{COMP}^3 - 31.278 \cdot V_{COMP}^2 + 42.384 \cdot V_{COMP} - 20.642\right)}{T_{ON}+T_{OFF}} \quad [16]$$

V_{COMP} can be determined by extrapolating from Figure 7 according to the on-time operating point.

$$\frac{V_{OUT}(s)}{V_{COMP}(s)} = \frac{\delta d}{\delta V_{COMP}} \cdot \frac{V_{IN(RMS)}}{\sqrt{k}} \cdot \frac{1}{1+\left(\frac{s \cdot R_{LOAD} \cdot C_{OUT}}{2}\right)} \quad [17]$$

By combining all of the above equations, the plant small-signal transfer function can be determined for a given set of conditions. From there the bode plot can be generated for the control to output power conversion stage, which is valid for the specified operating point.

The DEMO_100W_24VDC_FB board includes secondary-side voltage and current feedback loops ORed together through D6 and D9 to provide a current sink for the diode of the opto-isolator IC2. During normal operation only the voltage feedback loop is in operation. The current feedback loop is included for over-load and short-circuit protection only. In both cases accurate temperature stable references are derived from IC4, being divided via R47 and R49 to provide the current feedback reference. The output current is sensed through the parallel shunt resistor combination including RCS1, RCS2 and RCS3.

Stable operation over the range of line and load depends on the correct compensation of the voltage feedback loop, which is constructed around the operational amplifier IC5A. The output voltage is scaled to the 2.5 V reference provided by IC4, through the divider network of R35 and R38. As the ouput voltage starts to rise above 24 V, the voltage at the divider node of R35 and R38 reaches the 2.5 V threshold and the output of IC5A (pin 1) sinks more current increasing the current through the opto diode. The opto-transistor therefore pulls down on the IRS2982 COMP input to reduce the on-time, which makes the output voltage fall.

The voltage feedback loop transfer function G(s) is composed of the error amplifier E(s) and the opto-isolator and COMP pin network I(s):

$$G(s) = E(s) \cdot I(s) \quad [18]$$

where

$$E(s) = \frac{\left(R30 - \frac{1}{s \cdot C30}\right)}{\left(s \cdot R30 \cdot C28 + \frac{C28}{C3} + 1\right) \cdot R35} \quad [19]$$

and

$$I(s) = \frac{CTR \cdot R3}{R32 \cdot (1 + s \cdot C2 \cdot R3)} \quad [20]$$

Where CTR is the current transfer ratio of the opto-isolator.

E(s) is simplified since C28 is not fitted to the board, therefore

$$E(s) = \frac{\left(R30 - \frac{1}{s \cdot C30}\right)}{R3} \quad [21]$$

The combined voltage feedback loop transfer function then takes the form:

$$G(s) = \frac{V_{COMP}(s)}{V_{OUT}(s)} = -CTR \cdot \frac{R_{31}}{R_{32}} \cdot \frac{R_{30}}{R_{35}} \cdot \frac{1 + \frac{s}{\omega_{Z0}}}{\left(1 + \frac{s}{\omega_{p1}}\right)} \quad [22]$$

In order for the converter to provide high power factor and low iTHD the voltage loop response must be slow enough for the on-time to remain effectively constant throughout each line frequency half-cycle. Since the AC-line frequency is 50 to 60 Hz the overall gain then needs to roll off at a lower frequency. Since the load variation is wide it is challenging to keep the crossover frequency less than 10 Hz and have a good phase margin.

The equation above shows how the DC gain can be adjusted via R30, R31, R32 and R35. However R35 is fixed as part of the divider and R32 needs be selected to supply the opto-isolator diode with a current in the milliamp range, therefore adjustment is made with R30 and R31. It can be seen that adjusting these values also moves the pole and zero frequencies so C22 and C30 must be adjusted to position them as needed. It can be seen that C22 needs to be large enough for the pole to exist at around 10 Hz.

Based on the circuit values: ω_{P1} = 77 rads/s, 12.3 Hz and ω_{Z1} = 50 rads/s, 8 Hz.

These are positioned to provide a large phase margin calculated at around 75 degrees at maximum load, which gets smaller as the load is reduced, reaching 50 degrees at 10 percent load and dropping further at lighter loads. These values are calculated using a MathCAD script that calculates and the closed loop gain and phase. This tool is sufficient to demonstrate that the gain will cross over at the desired frequency close to 10 Hz at full load, dropping to 2 Hz at 10 percent load. It can be seen that the system will remain stable over the load range although the dynamic response will be quite slow. This cannot be avoided in a single-stage PFC Flyback converter.

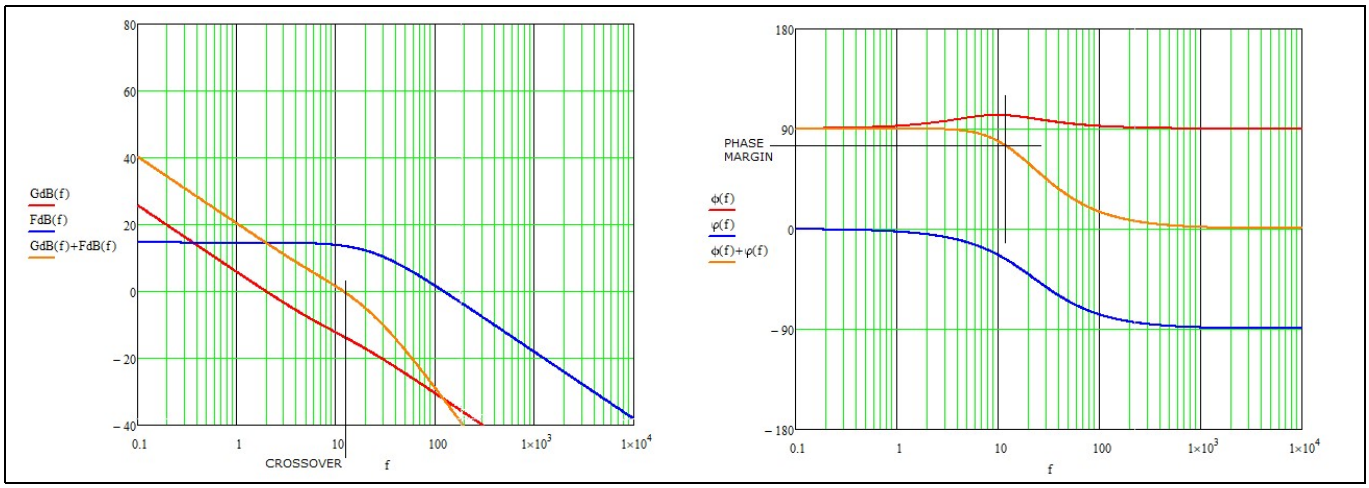


Figure 13 System gain (left) and phase (right) response at full-load, low-line voltage

7.2 Output capacitor calculation

The selection of the output capacitor is based on low-frequency 120 Hz ripple and the ESR. The output capacitor (C_{OUT}) can be a parallel combination of four capacitors to reduce the low-frequency ripple and the ESR.

$$C_{OUT} = \frac{P_{OUT}}{2 \cdot \pi \cdot f_{IN(MIN)} \cdot \Delta_{RIPPLE} \cdot V_{OUT}^2} \quad [F] \quad [23]$$

$$= \frac{100.8}{2 \cdot \pi \cdot 50 \cdot 2 \cdot 24^2} = 279\ \mu F$$

$$ESR \leq \frac{V_{RIPPLE}}{I_{SEC(PK)}}$$

$$= \frac{2V}{20A} = 100 m\Omega$$

$$I_{SPK} = 2 \cdot \frac{I_{OUT}}{(1 - D_{max})} = \frac{2 \cdot 4.2}{(1 - 0.58)} = 20\ A$$

$$I_{SRMS} = I_{SPK} \cdot \sqrt{\frac{1 - D_{max}}{3}} = 20 \cdot \sqrt{\frac{1 - 0.58}{3}} = 7.483\ A$$

$$I_{COUT(RMS)} = \sqrt{I_{SRMS}^2 - I_{OUT}^2} = \sqrt{7.483^2 - 4.2^2} = 6.194\ A$$

Three capacitors each of value 1200 μF (part number: 860040580016) are selected. Each capacitor has 2.8 A ripple current capability at 100 kHz and an ESR equal to 28 mΩ.

7.3 MOT resistor calculation for IR1161L

The MOT is linear in relation to the resistor value R_{MOT}. The following formula can be used to determine the required value:

$$R_{MOT} = 5.10^{10} \cdot t_{MOT} \quad [24]$$

The value of R_{MOT} should not be lower than the minimum recommended on the datasheet. On this board a standard value of 39 kΩ is used at the MOT pin of the IC. This value gives a minimum on-time of 780 ns.

8 Protection features

8.1 Brown-out protection

The following circuit has been used to implement the brown-out protection of the PFC Flyback converter. The converter stops switching once the input AC voltage falls below 60 to 65 V_{RMS} and turns back on when the input AC voltage rises above 85 to 90 V_{RMS}. When the input to IC3 divided from the rectified input voltage V DC through the network consisting of R29, R33, R36, R40 and R42 rises above the 2.5 V threshold, the cathode of DZ4 is pulled down to 2.5 V. This causes Q1 to switch off, allowing COMP1 to start and the converter to start up. In this state D8 is blocking and R42 forms part of the divider network. If the AC input voltage falls below 60 to 65 V_{RMS} the input to IC3 falls below 2.5 V and the cathode voltage rises until DZ4 conducts and Q1 is turned on. At this point D8 conducts, pulling down on the node of R40 and R42 thereby adjusting the divider ratio to provide hyteresis requiring a higher AC input and VDC voltage to 2.5 V at the IC3 input required to pull down the cathode and turn off Q1 again.

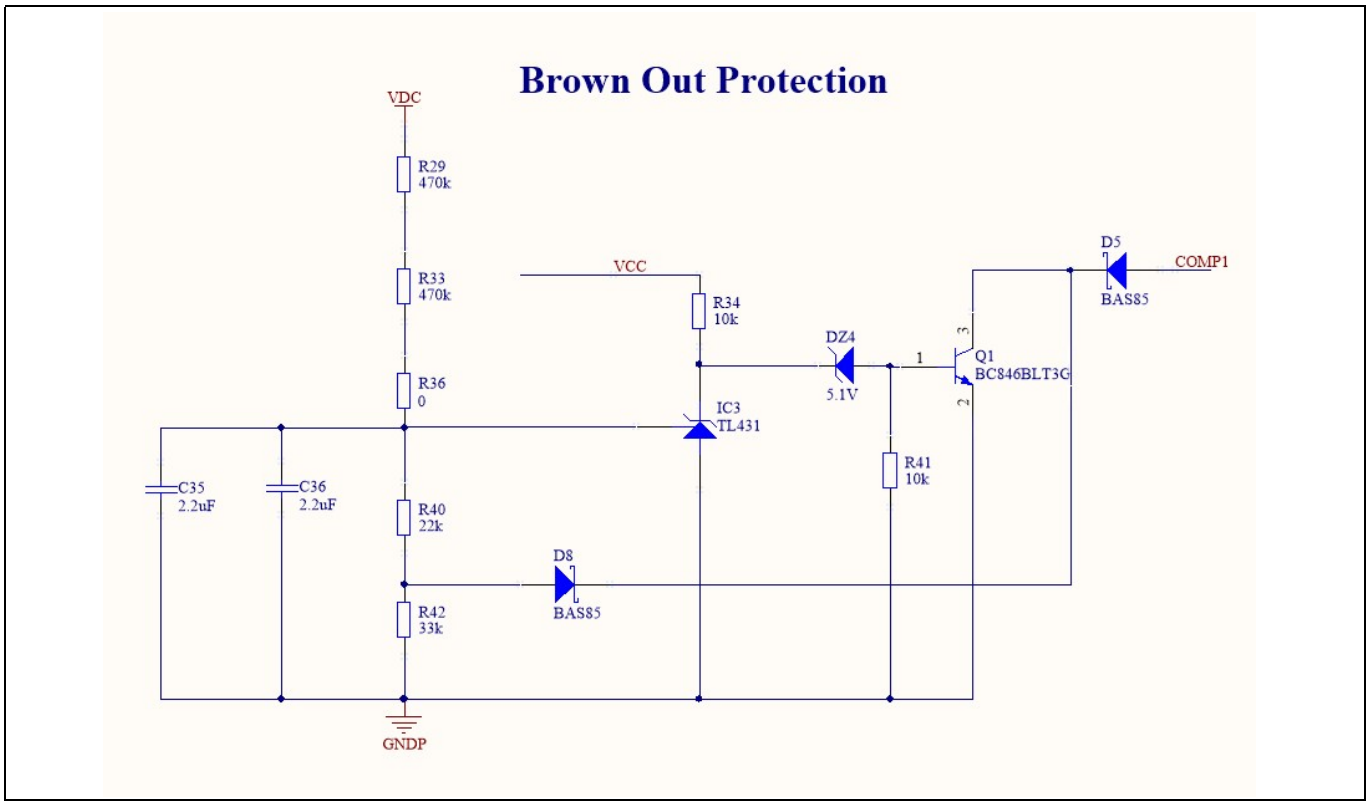


Figure 14 Brown-out protection circuit

8.2 Overload and short-circuit protection

The over-current protection feature is very important in the flyback converter to prevent high currents occurring under a fault condition, which could result in failure of either the primary or secondary MOSFETs (M2 and M1). The primary cycle by cycle current limit provides some protection to M2 by terminating the gate drive if an excessive current is detected, however this alone is not sufficient to limit the output current and protect the power supply in the event of an overload or short-circuit.

To accomplish this an output current sensing network consisting of parallel resistors; Rcs1, Rcs2 and Rcs3 has been included. The voltage drop proportional to the output current is compared with a reference determined by the resistor divider R47 and R49 connected to the 2.5 V reference of IC4. IC5B is configured as a comparator with hysteresis determined by R43. If the sensed output current exceeds the reference the output transitions from high to low causing conduction through D9 to energize the feedback opto-isolator IC2. This causes the COMP voltage at IC1 to be pulled down rapidly as C22 is discharged, which turns off the gate drive to M2.

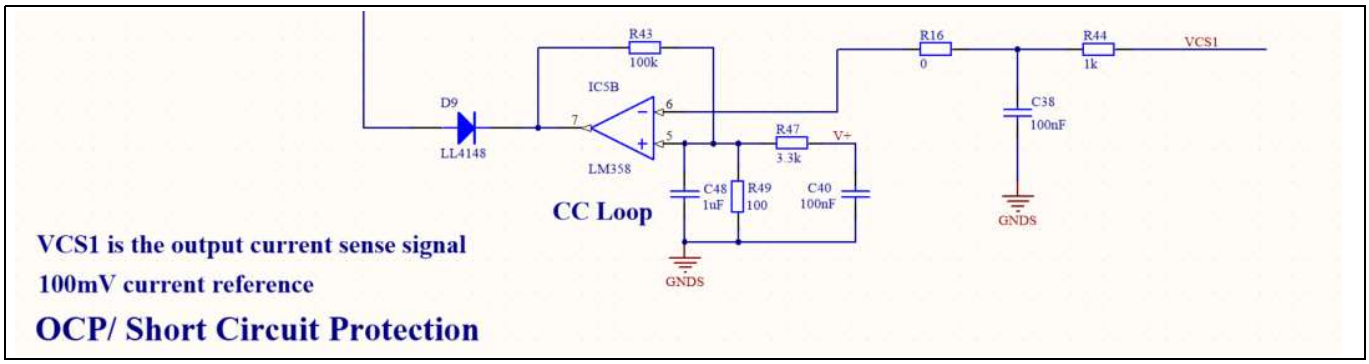


Figure 15 Overload and short-circuit protection circuit

Since the output current has now dropped to zero, the output of IC5B then transitions high shutting off the current through D9 and de-energizing IC2 allowing the system to re-start as C22 charges through R31. If the fault condition at the output remains then as the output current rises above the threshold the same shut down function will occur. This hiccup mode operation will continue indefinitely until the fault condition is removed allowing the power supply to automatically re-start.

9 Bill of Materials (BOM)

Designator	Manufacturer	Part Number	Quantity	Value/Rating
BR1	Vishay Semiconductor Diodes Division	GBU4J-E3/51	1	600 V/4 A/4-SIP/GBU
C2, C3, C4, C25	Samsung Electro-Mechanics	CL10B104KB8NNNL	4	0.1 µF/50 V/X7R/0603
C8, C39	Kemet	C1210C104KBRAC7800	2	0.1 µF/630 V/X7R/1210
C9, C10	Wurth Electronics Inc.	890334023028	2	0.22 µF/310 VAC/Radial/10%
C11	EPCOS (TDK)	B32621A6222K189	1	2.2 nF/630 V
C12	Kemet	C330C222GDG5TA	1	2.2 nF/1 kV/NP0/Radial
C13	Yageo	CC1206KRX7RABB102	1	1 nF/200 V/X7R/1206
C14, C15, C27	Panasonic Electronic Components	ECQ-U3A104MG	3	0.1 µF/300 VAC/20%/Radial
C16, C17, C20, C32, C44, C45, C47	Vishay, Vishay BC Components	VY1102M29Y5VQ6TV0	7	1 nF/500 VAC/Y5V Radial
C18	Wurth Electronics Inc.	885012208058	1	0.1 µF/25 V/X7R/1206
C19	Rubycon	50YXG220MEFC10X16	1	220 µF/50 V/20%/Radial
C21	TDK Corporation	CGA3E2NP01H220J080AA	1	22 pF/50 V/NP0/0603
C22	Kemet	C1206C105J3RACTU	1	1 µF/25 V/X7R/1206
C23	Wurth Electronics Inc.	860160474016	1	180 µF/25 V/20%
C24	Wurth Electronics Inc.	885012007040	1	1 nF/25 V/C0G/NP0/0805
C26	Samsung Electro-Mechanics	CL31B106KAHNNNE	1	10 µF/25 V/X7R/1206
C28			1	
C29	Yageo	CC0603JRNPOYBN151	1	150 pF/250 V/NPO/0603
C30, C35, C36	Yageo	CC1206JKX7R8BB225	3	2.2 µF/25 V/X7R/1206
C33, C38, C40	AVX	08053C104JAT2A	3	0.1µF/25V/0805/5%
C34	Kemet	C0805C106K8PACTU	1	10µF/10V/X5R/0805
C48	AVX Corporation	08053C105JAT2A	1	1 µF/25 V/X7R/0805
C41, Cx	Wurth Electronics Inc.	890334024005	2	0.47 µF/310 VAC/10%/Radial
C42	Kemet	C0805C471JDRACTU	1	470 pF/1 kV/ X7R/0805
C43	Wurth Electronics Inc.	860040572002	1	47 µF/35 V/20%

CO1, CO2, CO3	Wurth Electronics Inc.	860040580016	3	1200 µF/35 V
COMP1, ZX1	Keystone	5004	2	0.04" dia yellow
D1	Diodes Inc	RS3K-13-F	1	800 V/3 A/SMC
D2, D3, D4, D6, D7, D9, D77, D78, D79, D80	ON Semiconductor	FDLL4148	10	100 V/0.2 A/MINIMELF
D5, D8	Vishay	BAS85-GS08	2	Schottky/30 V/200 mA/SOD80
DZ1	Nexperia USA Inc.	BZV55-C12,115	1	Zener/12 V/500 mW/SOD80C
DZ2	Nexperia USA Inc.	BZV55-C16,115	1	Zener/16V/500mW/SOD80C
DZ3	Nexperia USA Inc.	BZV55-C3V9,115	1	Zener/3.9 V/500 mW/SOD80C
DZ4	Nexperia USA Inc.	BZV55-C5V1,115	1	Zener/5.1 V/500 mW/SOD80C
DZ5	Micro Commercial Co	P6KE250A-TP	1	TVS DIODE/214 V/344 V/DO15
DZ6	Nexperia USA Inc.	BZV55-C24,115	1	Zener/24V/500mW/SOD80C
IC1	Infineon	IRS2982S	1	SMPS Controller
IC2	Vishay Semiconductor Opto Division	SFH6286-2T	1	Opto-isolaror/5.3 kV/TRANS/4-SMD
IC3, IC4	Diodes Inc	ZTL431AFTA	2	Voltage Reference/SOT23-3
IC5	Diodes Inc	LM358S-13	1	Operational amplifier/dual
L1	Wurth Electronik	750317969	1	Flyback
L2, L4, L5, L7	Bourns	2124-V-RC	4	1 mH/1.3 A
L3, L6	TDK	B82733F2122B1	2	CM choke 39 mH/1.2 A
M1	Infineon	IRFS4321	1	150 V/60 A/15 mΩ/D2PAK
M2	Infineon	IPA80R280P7	1	800 V/17 A/280 mΩ/TO-220
P1	Phoenix Contact	1985195	1	2 Position/3.5mm/Green
P2	Phoenix Contact	1985205	1	3 Position/3.5mm/Green
Q1, Q2, Q3	ON Semiconductor	BC846BLT3G	3	NPN/65V/0.1A/SOT-23
R1	Yageo	CFR-50JB-52-10K	1	10 k/0.5 W/5%
R2, R3	Stackpole Electronics Inc.	RSF2JT10R0	2	10/2 W/5%/Axial
R4, R5, R12	Yageo	FMP200FRF52-130K	3	130 k/2 W/1%/Axial
R6, R7, R8	Stackpole Electronics Inc.	CR1206-JW-151ELF	3	150/0.25 W/1206/5%
R9, R11	Yageo	RC1206FR-076K2L	2	6.2 k/0/25 W/1206/1%
R10	Yageo	RC1206FR-0714KL	1	14 k/0.25 W/1206/1%
R13, R45	Panasonic Electronic Components	ERJ-8ENF1002V	2	10 k/0.25 W/1206/1%

R14	TDK	B57153S479M54	1	ICL/4.7 Ω/3 A/20%/8.5 mm
R15, R19	Vishay Dale	CRCW12061R00FKEA	2	1/0.25 W/1206/1%
R16	Stackpole Electronics	RMCF0805ZT0R00	1	0/0.125 W/0805
R17, R25, R26, R48, R50, R51, R52	Panasonic Electronic Components	ERJ-8GEYJ682V	7	6.8 k/0.25 W/1206/5%
R18	Yageo	RC0805FR-07470RL	1	470/0.125 W/0805/1%
R20, R21, R22, R23, R24, R46	Vishay Dale	CRCW12061R00FKEA	6	1/0.25 W/1206/1%
R27, R44	TE Connectivity Passive Product	CRG1206F1K0	2	1 k/0.25 W/1206/1%
R28	Stackpole Electronics Inc.	RMCF0805FT39K0	1	39 k/0.125 W/0805/1%
R29, R33	Yageo	RC1206FR-07470KL	2	470 k/0.25 W/1206/1%
R30	Yageo	RC0805FR-079K1L	1	9.1 k/0.125 W/0805/1%
R31	Yageo	RC1206FR-0713KL	1	13 k/0.25 W/1206/1%
R34, R41	Yageo	RC0805FR-0710KL	2	10 k/0.125 W/0805/1%
R35	Stackpole Electronics Inc.	RMCF1206FT1M00	1	1 M/0.25 W/1206/1%
R36	Stackpole Electronics Inc.	RMCF1206ZT0R00	1	0/0.25 W/1206
R37	Stackpole Electronics Inc.	RMCF0805FT2K70	1	2.7 k/0.125 W/0805/1%
R47	Stackpole Electronics Inc.	RMCF0805FT3K30	1	3.3 k/0.125 W/0805/1%
R32, R38	Vishay Dale	CRCW120610K0FKEAC	2	10 k/0.25 W/1206/1%
R39	Yageo	RC1206FR-0727KL	1	27 k/0.25 W/1206/1%
R40	Yageo	RC0805FR-0722KL	1	22 k/0.125 W/0805/1%
R42	Yageo	RC0805FR-0733KL	1	33 k/0.125 W/0805/1%
R43	TE Connectivity Passive Product	CRG0805F100K	1	100 k/0.125 W/0805/1%
R49	Yageo	RC0805FR-07100RL	1	100/0.125 W/0805/1%
R53	Stackpole Electronics Inc.	RMCF1206FT91K0	1	91 k/0.25 W/1206/1%
Rcs1, Rcs2, Rcs3	Yageo	RL2512FK-070R051L	3	51 mΩ/2512/1 W/1%
U1	Infineon	IR1161L	1	Synchronous Rectifier IC /SOT23-5
VCC1	Keystone	5000	1	0.04" dia red
VR1	EPCOS (TDK)	B72214S321K101	1	Varistor/510 V/4.5 kA/DISC/ 14 mm

10 PCB layout

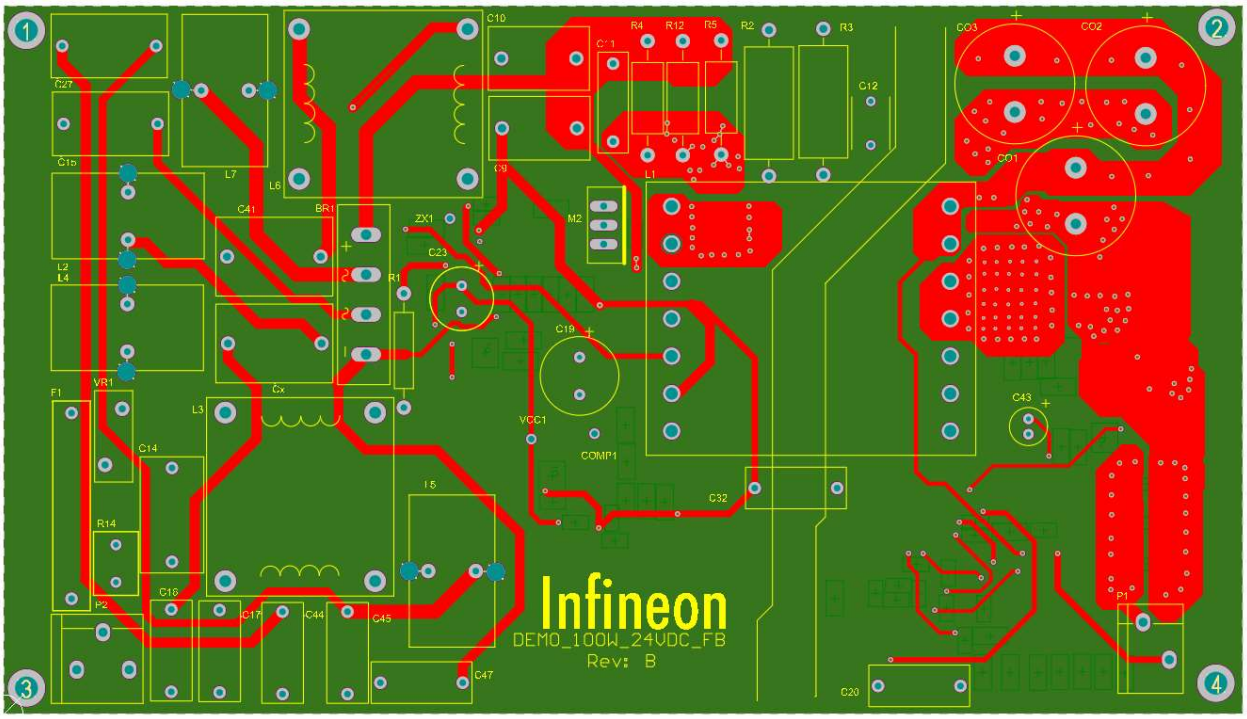


Figure 16 PCB top-side components and traces (top layer)

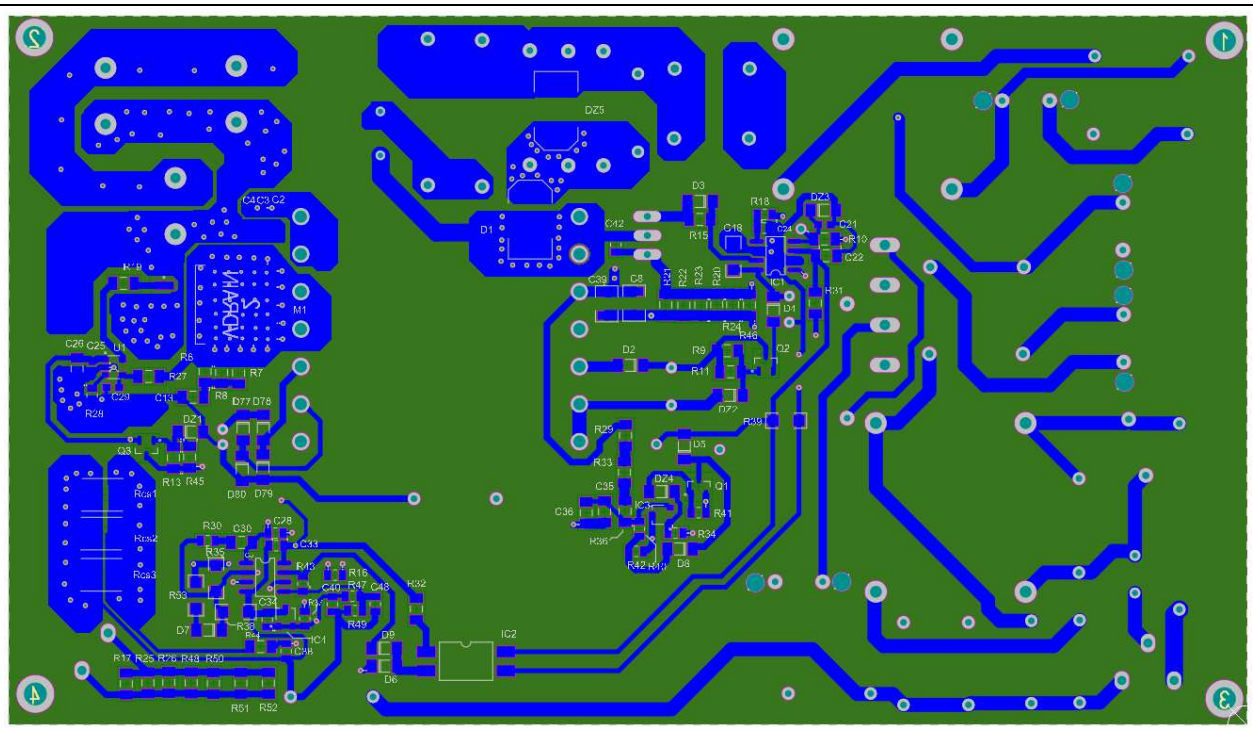


Figure 17 PCB bottom-side components and traces (bottom layer)

10.1 PCB layout guidelines for system optimization

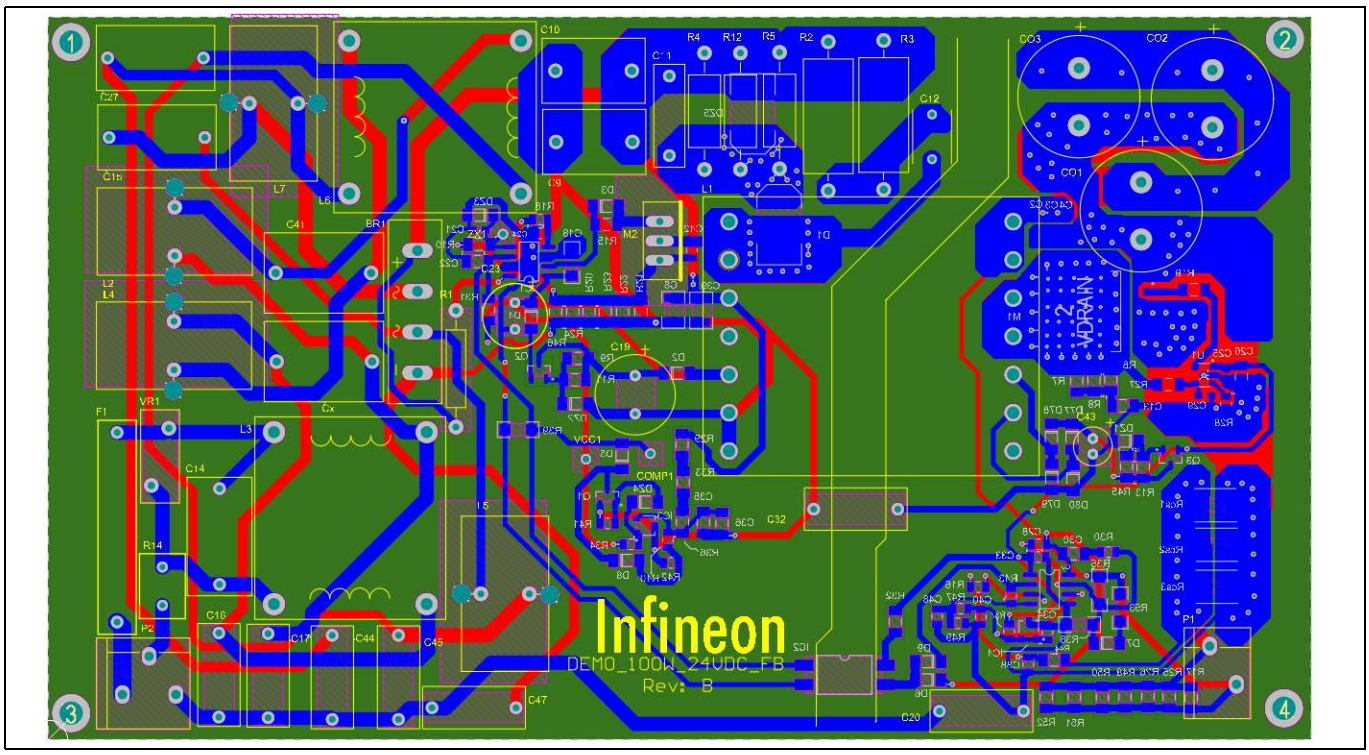


Figure 18 Complete board layout

The primary HF current loop on the left side of the board originates from HF capacitor C8 connecting to the Flyback inductor (L1). The other side of the Flyback inductor winding is connected to the drain of the MOSFET (M2) and the CS resistor R20. The other end of the CS resistor is connected to the return of the C8 capacitor. To minimize EMI and also the loop inductance, this HF loop is kept as small as possible.

The secondary-side HF current loop originates from C2, M1 and L1. Therefore, in order to keep the layout as tight as possible, these HF AC loop components are placed close to each other, minimizing the loop area, and this translates to lower EMI. In order to keep the loops as small as possible, it is preferable to use ceramic capacitors C2, C3 and C4 to close the AC loops and keep the return paths small. Aside from EMI considerations it is also extremely important to design the PCB so that IRS2982 and IR1161L ICs are able to operate correctly without suffering from potential interference caused by noise or incorrect grounding. Decoupling capacitors C18 and C25 are located right next to IC1 and U1 with direct connections to the V_{CC} and COM/0 V pins.

As in all switching power supplies, the signal and power grounds must be kept separate and join together only at the star points or single-point connections, which are at the negative side of the HF capacitor C8 for the primary side and C2 for the secondary side.

11 Flyback transformer specifications

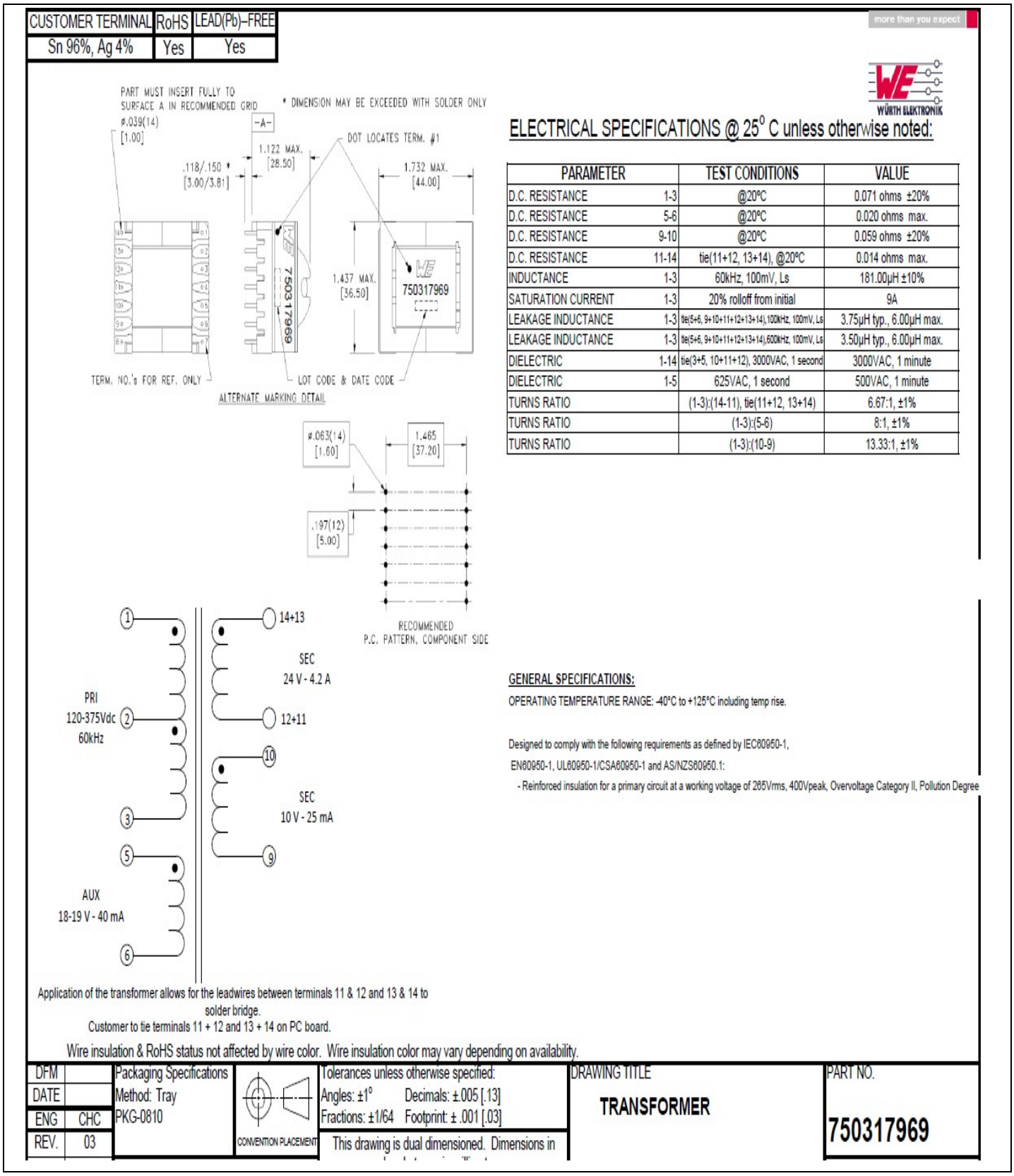


Figure 19 Flyback transformer

12 Test results

12.1 Operation under different line and load conditions

Table 2 Input 120 V $AC_{(RMS)}$

P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	PF	iTHD (%)	Efficiency (%)
1.64	23.95	0	0.00	0.25	---	0.00%
9.45	23.94	0.244	5.84	0.753	23.0%	61.81%
15.81	23.93	0.492	11.77	0.876	18.9%	74.47%
22.92	23.73	0.743	17.63	0.916	17.3%	76.93%
29.21	23.75	0.991	23.54	0.946	16.7%	80.58%
35.55	23.82	1.24	29.54	0.965	11.7%	83.09%
41.9	23.89	1.48	35.36	0.973	9.1%	84.38%
48.39	23.93	1.74	41.64	0.978	9.4%	86.05%
55	23.92	1.987	47.53	0.98	8.8%	86.42%
61.71	23.91	2.237	53.49	0.985	8.1%	86.67%
68.41	23.9	2.485	59.39	0.987	7.7%	86.82%
75.22	23.88	2.735	65.31	0.989	7.3%	86.83%
82.09	23.87	2.984	71.23	0.99	7.1%	86.77%
89.06	23.855	3.235	77.17	0.99	7.0%	86.65%
95.98	23.84	3.482	83.01	0.99	6.9%	86.49%
102.98	23.82	3.731	88.87	0.99	6.8%	86.30%
110.1	23.79	3.982	94.73	0.99	6.6%	86.04%
117.18	23.78	4.23	98.47	0.99	6.5%	85.84%

Table 3 Input 230 V AC$_{(RMS)}$

P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	PF	iTHD (%)	Efficiency (%)
1.8	23.9	0	0.00	0.08	---	0.00%
9.77	23.85	0.244	5.82	0.35	---	59.56%
16.96	23.85	0.492	11.73	0.53	22.4%	69.19%
23.6	23.67	0.742	17.56	0.65	19.0%	74.42%
30.17	23.63	0.99	22.80	0.73	19.0%	77.54%
36.31	23.57	1.241	28.63	0.78	17.4%	80.56%
42.7	23.42	1.489	34.87	0.83	15.4%	81.67%
49.23	23.63	1.739	41.09	0.87	14.0%	83.47%
55.6	23.73	1.988	47.18	0.89	13.3%	84.85%
62.12	23.76	2.237	53.15	0.91	13.0%	85.56%
68.45	23.75	2.485	59.02	0.92	13.2%	86.22%
74.89	23.75	2.735	64.96	0.93	13.0%	86.74%
81.32	23.75	2.984	70.87	0.94	12.7%	87.15%
87.83	23.73	3.234	76.74	0.94	13.1%	87.38%
94.28	23.73	3.482	82.63	0.95	13.4%	87.64%
100.77	23.72	3.731	88.50	0.952	13.7%	87.82%
107.39	23.71	3.981	94.39	0.96	14.0%	87.89%
114	23.71	4.229	100.27	0.96	14.0%	87.96%

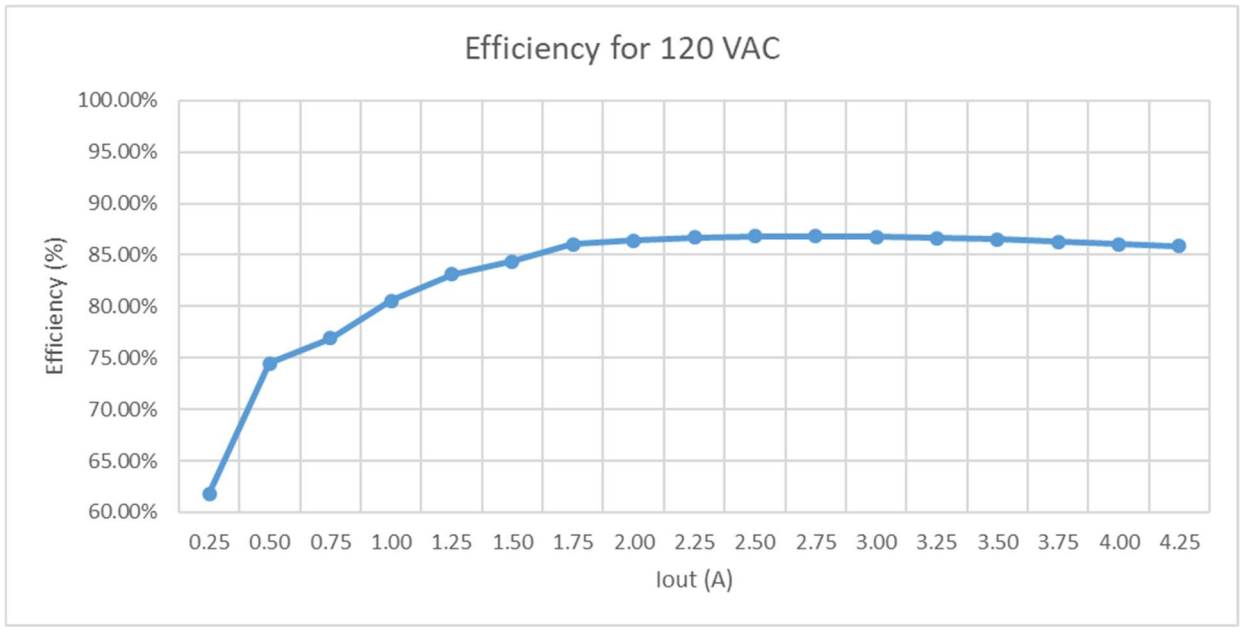


Figure 20 Efficiency at 120 V AC_{RMS} input

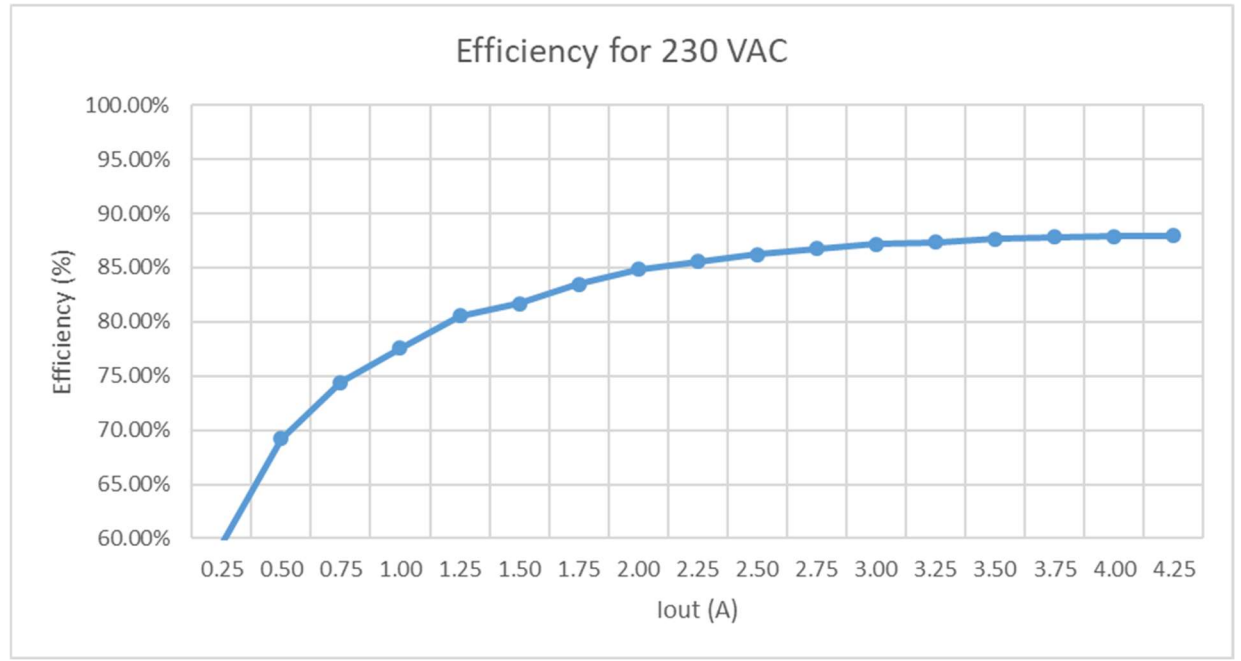


Figure 21 Efficiency at 230 V AC_{RMS} input

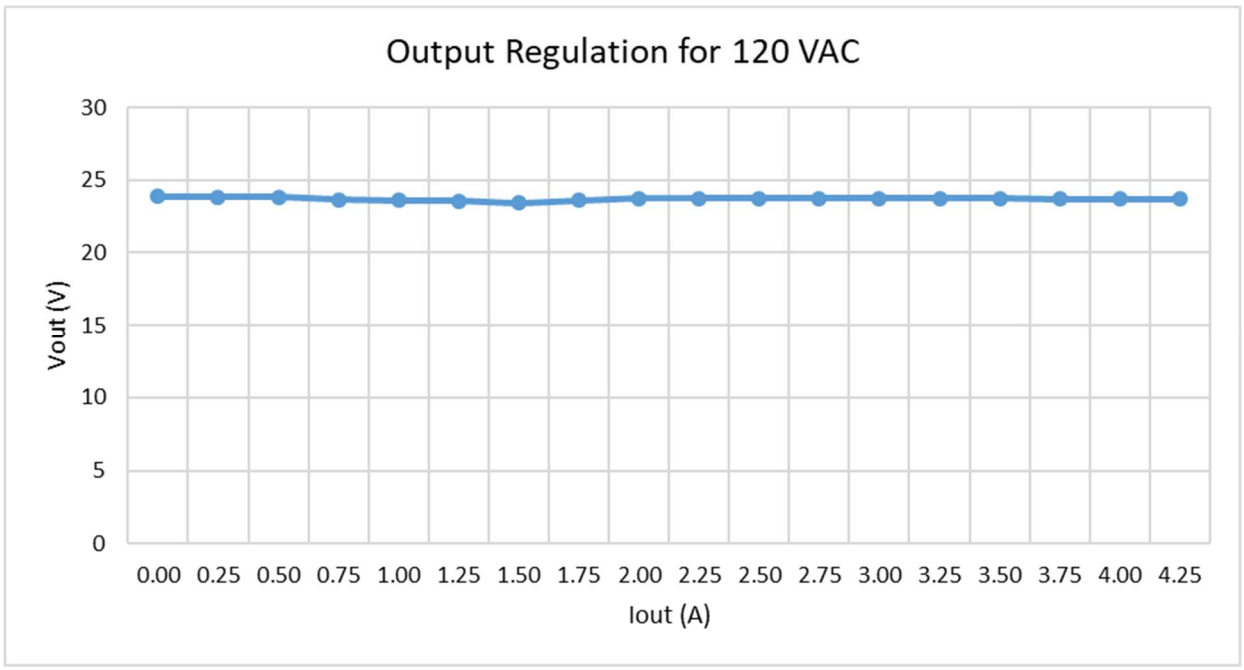


Figure 22 Load regulation at 120 V AC_{RMS} input

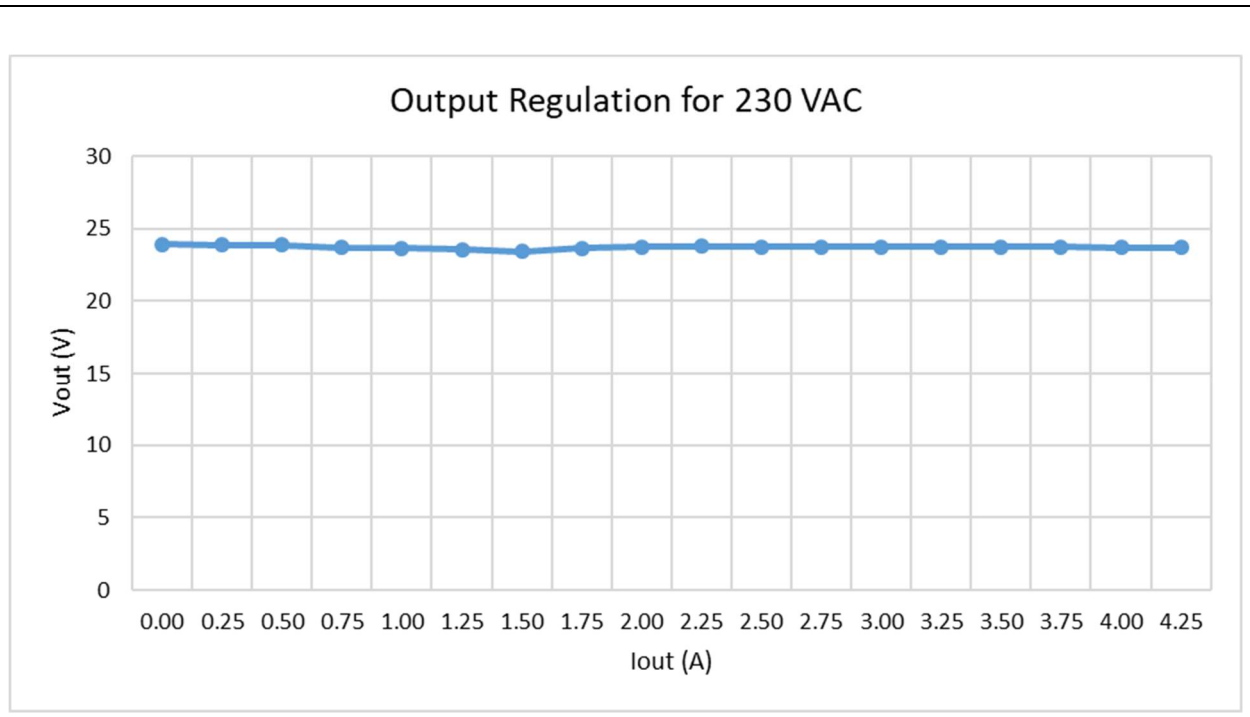


Figure 23 Load regulation at 230 V AC_{RMS} input

12.2 Power factor and input current harmonics (iTHD)

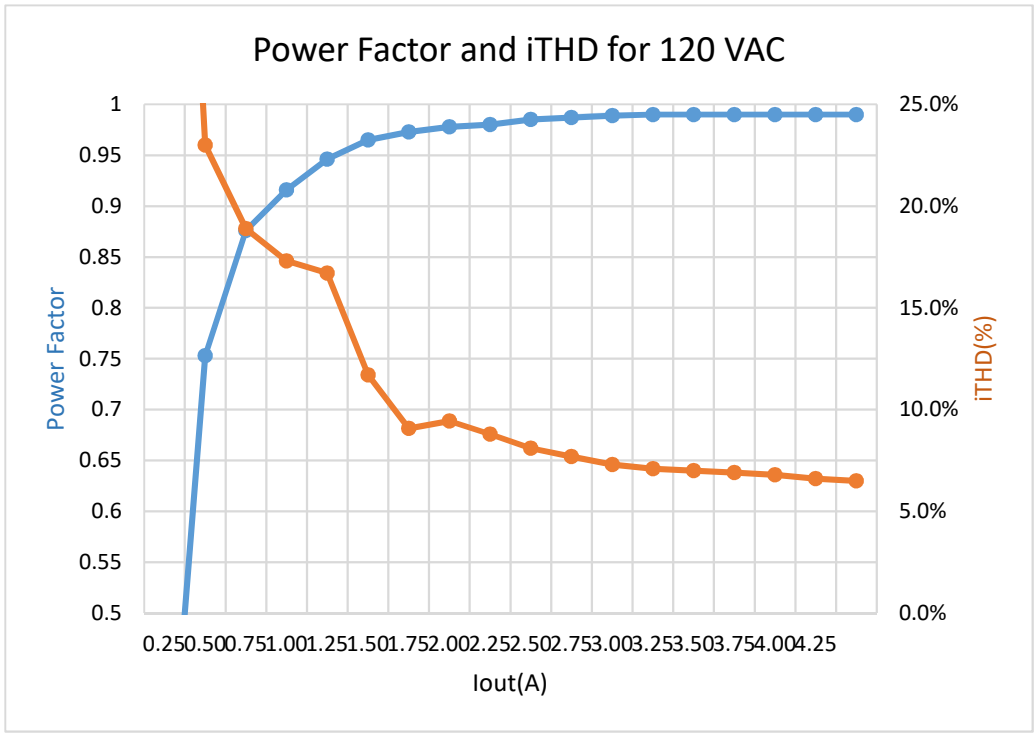


Figure 24 Power factor and iTHD at 120 V AC_{RMS} input

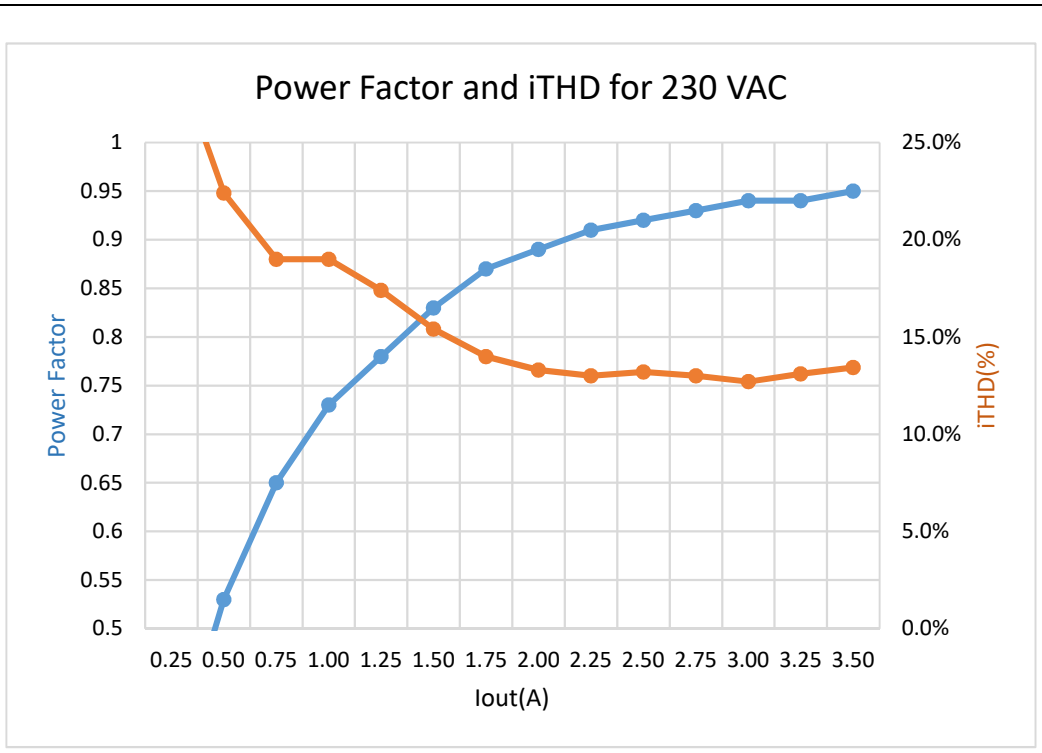
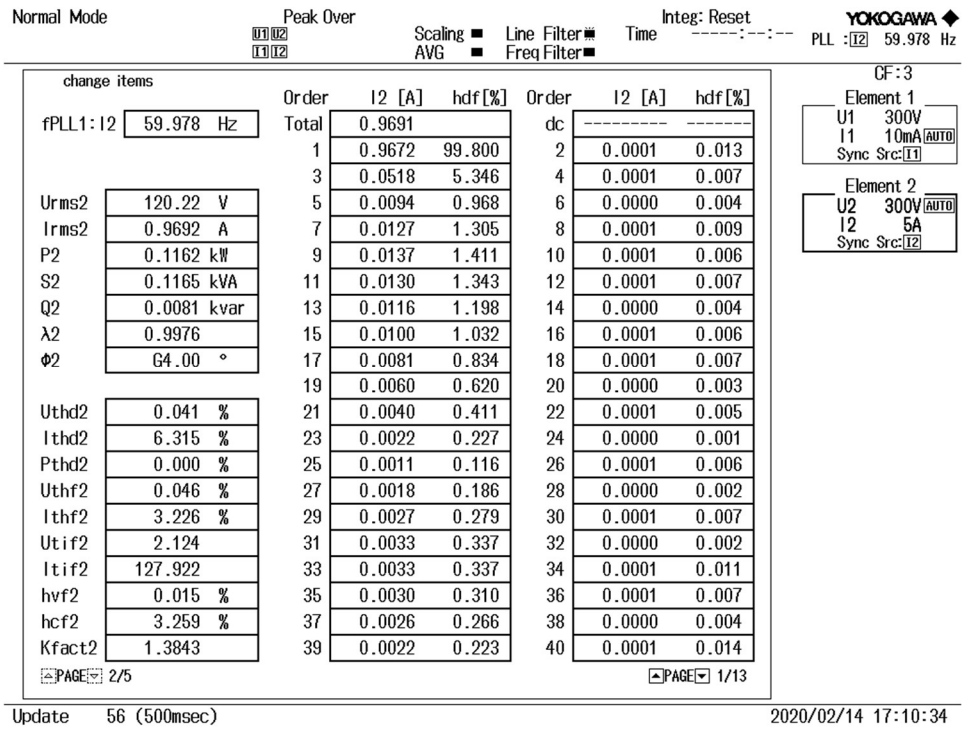


Figure 25 Power factor and iTHD at 230 V AC_{RMS} input

An international standard, the IEC 1000-3-2 (EN 61000-3-2), defines the rules for the current distortion affecting mains-powered devices. This standard does not discuss the power factor directly but fixes current harmonic limits [4].

Table 4 EN 61000-3-2 class D limits for system power greater than 75 W

	Harmonics limits class D according to EN 61000-3-2 for system power greater than 75 W and less than 600 W	
	Harmonics order n	**mA_{RMS}/W**
Requirements	3	3.4
	5	1.9
	7	1.0
	9	0.5
	11	0.35
	13	0.296
	15 less than or equal to n less than or equal to 39	3.85/n



Normal Mode | Peak Over U1 U2 I1 I2 | Scaling ■ AVG ■ | Line Filter ■ Freq Filter ■ | Time -----:--:-- | Integ: Reset | YOKOGAWA ◆ PLL :I2 59.978 Hz

change items

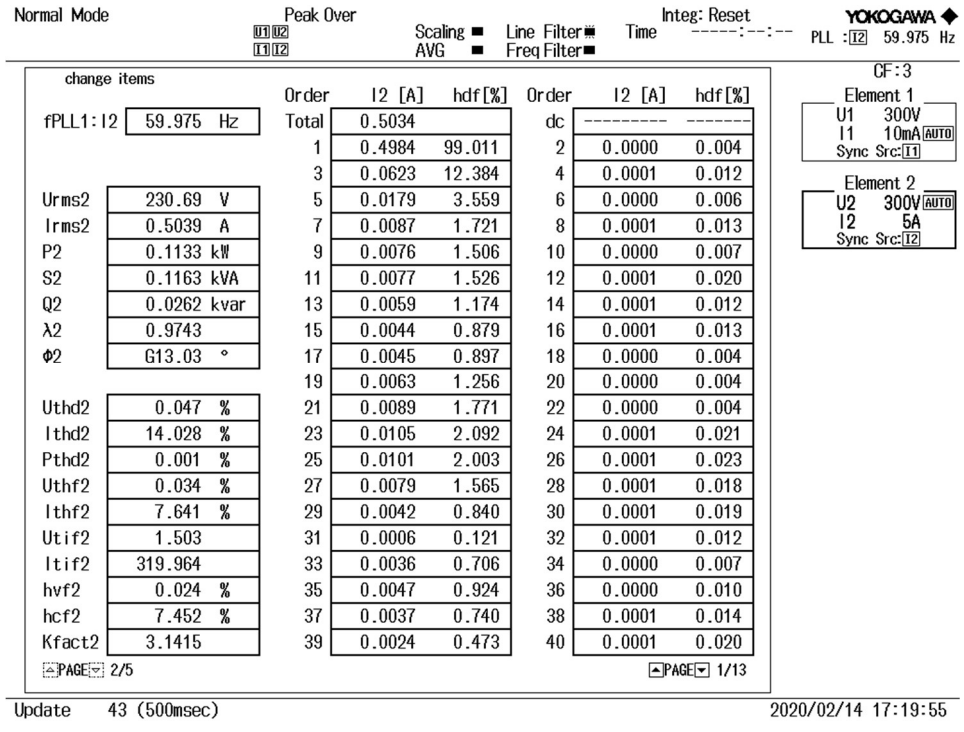
		Order	I2 [A]	hdf[%]	Order	I2 [A]	hdf[%]
fPLL1:I2	59.978 Hz	Total	0.9691		dc	---------	------
		1	0.9672	99.800	2	0.0001	0.013
		3	0.0518	5.346	4	0.0001	0.007
Urms2	120.22 V	5	0.0094	0.968	6	0.0000	0.004
Irms2	0.9692 A	7	0.0127	1.305	8	0.0001	0.009
P2	0.1162 kW	9	0.0137	1.411	10	0.0001	0.006
S2	0.1165 kVA	11	0.0130	1.343	12	0.0001	0.007
Q2	0.0081 kvar	13	0.0116	1.198	14	0.0000	0.004
λ2	0.9976	15	0.0100	1.032	16	0.0001	0.006
Φ2	G4.00 °	17	0.0081	0.834	18	0.0001	0.007
		19	0.0060	0.620	20	0.0000	0.003
Uthd2	0.041 %	21	0.0040	0.411	22	0.0001	0.005
Ithd2	6.315 %	23	0.0022	0.227	24	0.0000	0.001
Pthd2	0.000 %	25	0.0011	0.116	26	0.0001	0.006
Uthf2	0.046 %	27	0.0018	0.186	28	0.0000	0.002
Ithf2	3.226 %	29	0.0027	0.279	30	0.0001	0.007
Utif2	2.124	31	0.0033	0.337	32	0.0000	0.002
Itif2	127.922	33	0.0033	0.337	34	0.0001	0.011
hvf2	0.015 %	35	0.0030	0.310	36	0.0001	0.007
hcf2	3.259 %	37	0.0026	0.266	38	0.0000	0.004
Kfact2	1.3843	39	0.0022	0.223	40	0.0001	0.014

PAGE 2/5 | PAGE 1/13

CF:3
Element 1: U1 300V, I1 10mA AUTO, Sync Src:I1
Element 2: U2 300V AUTO, I2 5A, Sync Src:I2

Update 56 (500msec) | 2020/02/14 17:10:34

Figure 26 Power analyzer read-out at 120 V AC_{RMS} input with 4.2 A load



Normal Mode | Peak Over U1 U2 I1 I2 | Scaling ■ AVG ■ | Line Filter ■ Freq Filter ■ | Time -----:--:-- | Integ: Reset | YOKOGAWA ◆ PLL :I2 59.975 Hz

change items

		Order	I2 [A]	hdf[%]	Order	I2 [A]	hdf[%]
fPLL1:I2	59.975 Hz	Total	0.5034		dc	---------	------
		1	0.4984	99.011	2	0.0000	0.004
		3	0.0623	12.384	4	0.0001	0.012
Urms2	230.69 V	5	0.0179	3.559	6	0.0000	0.006
Irms2	0.5039 A	7	0.0087	1.721	8	0.0001	0.013
P2	0.1133 kW	9	0.0076	1.506	10	0.0000	0.007
S2	0.1163 kVA	11	0.0077	1.526	12	0.0001	0.020
Q2	0.0262 kvar	13	0.0059	1.174	14	0.0001	0.012
λ2	0.9743	15	0.0044	0.879	16	0.0001	0.013
Φ2	G13.03 °	17	0.0045	0.897	18	0.0000	0.004
		19	0.0063	1.256	20	0.0000	0.004
Uthd2	0.047 %	21	0.0089	1.771	22	0.0000	0.004
Ithd2	14.028 %	23	0.0105	2.092	24	0.0001	0.021
Pthd2	0.001 %	25	0.0101	2.003	26	0.0001	0.023
Uthf2	0.034 %	27	0.0079	1.565	28	0.0001	0.018
Ithf2	7.641 %	29	0.0042	0.840	30	0.0001	0.019
Utif2	1.503	31	0.0006	0.121	32	0.0001	0.012
Itif2	319.964	33	0.0036	0.706	34	0.0000	0.007
hvf2	0.024 %	35	0.0047	0.924	36	0.0000	0.010
hcf2	7.452 %	37	0.0037	0.740	38	0.0001	0.014
Kfact2	3.1415	39	0.0024	0.473	40	0.0001	0.020

PAGE 2/5 | PAGE 1/13

CF:3
Element 1: U1 300V, I1 10mA AUTO, Sync Src:I1
Element 2: U2 300V AUTO, I2 5A, Sync Src:I2

Update 43 (500msec) | 2020/02/14 17:19:55

Figure 27 Power analyzer read-out at 230 V AC_{RMS} input with 4.2 A load

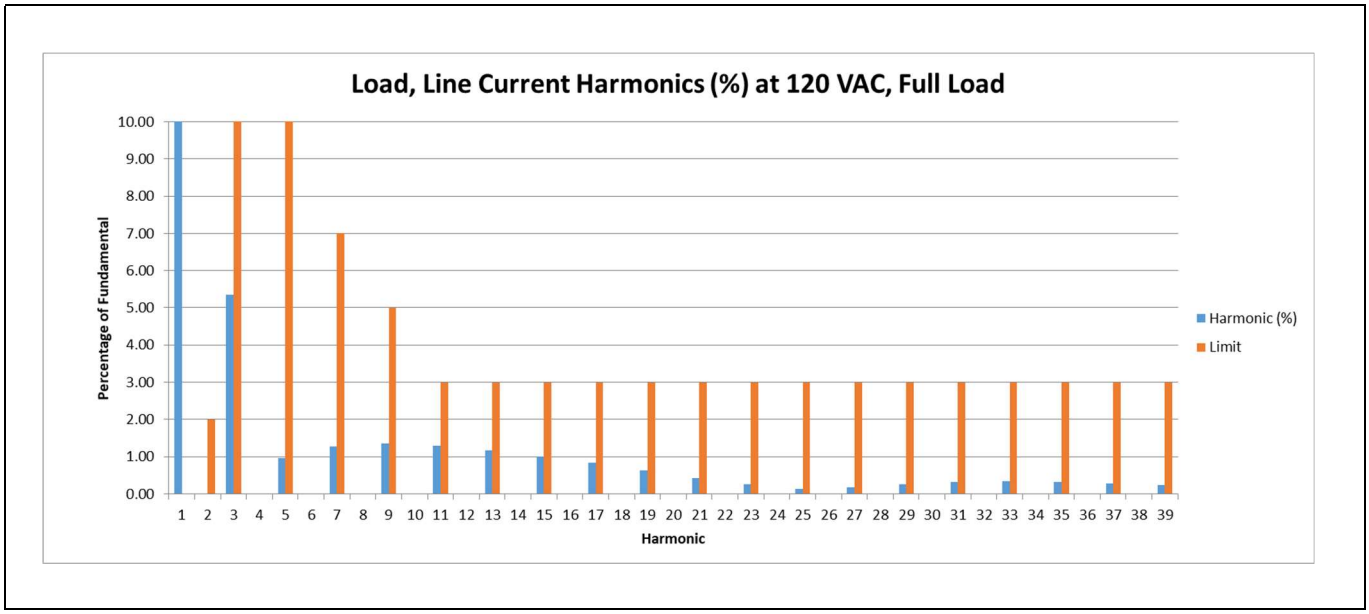


Figure 28 Input current harmonics compared with class D limits at 120 V AC_{RMS} input with 4.2 A load

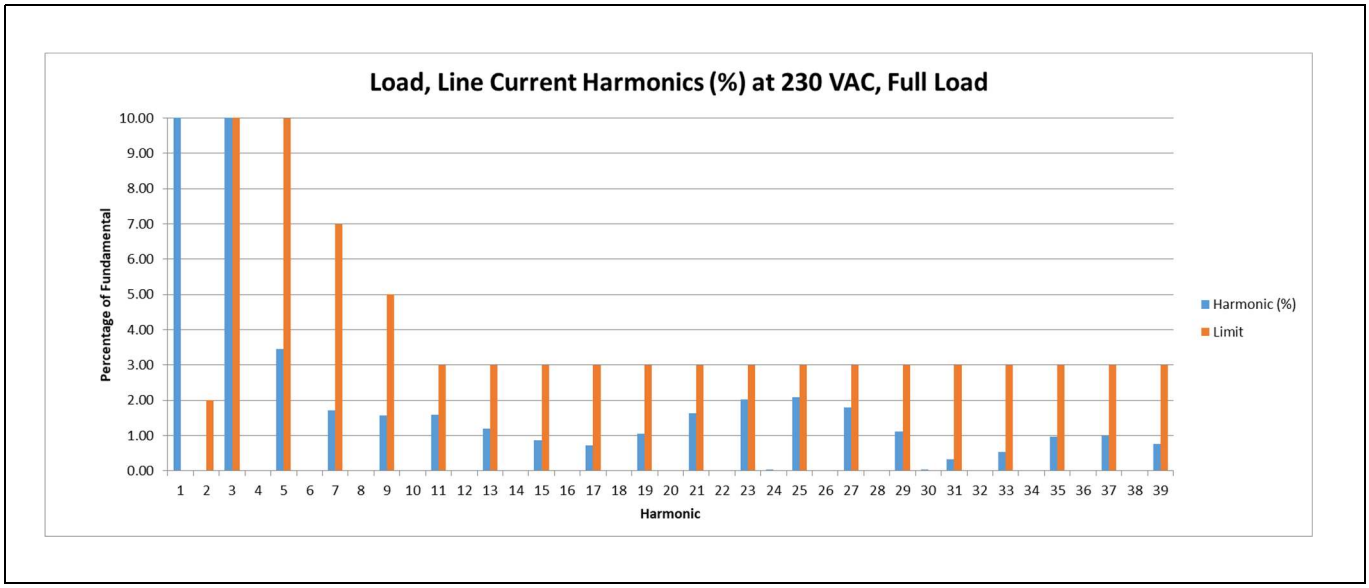


Figure 29 Input current harmonics compared with class D limits at 230 V AC_{RMS} input with 4.2 A load

It is shown that the input current harmonics at full load are well within the class D limits of standard EN 61000-3-2 at both nominal input voltages.

12.1 Operating waveforms

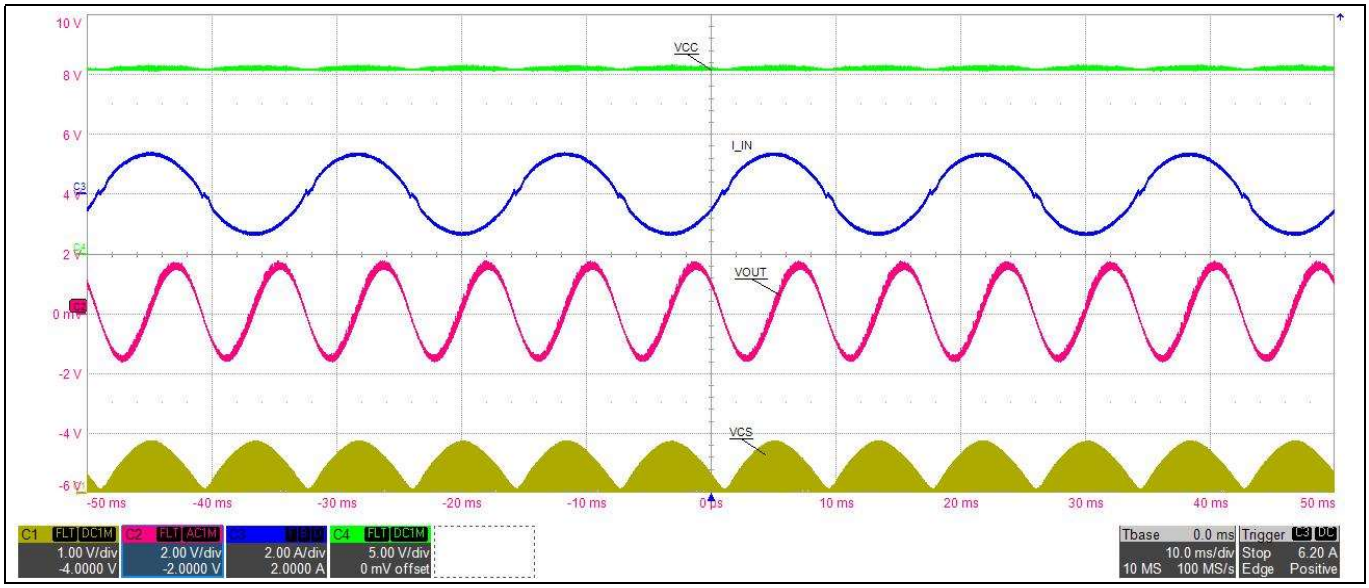


Figure 30 **120 V AC_{RMS} steady-state operation at 100 percent load: output voltage V_{OUT} ripple (red), input current (blue), current sense V_{CS} (yellow), V_{CC} (green)**

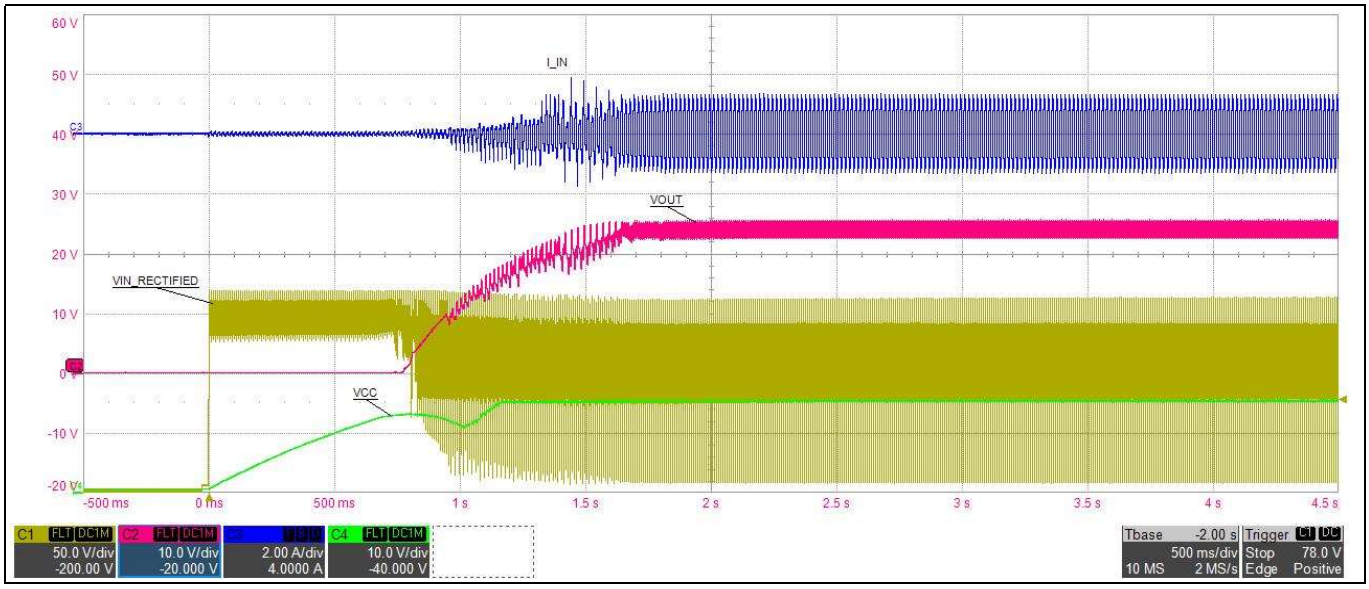


Figure 31 **120 V AC_{RMS} start-up operation at 100 percent load: output voltage V_{OUT} (red), input current (blue), rectified input voltage (yellow), V_{CC} (green)**

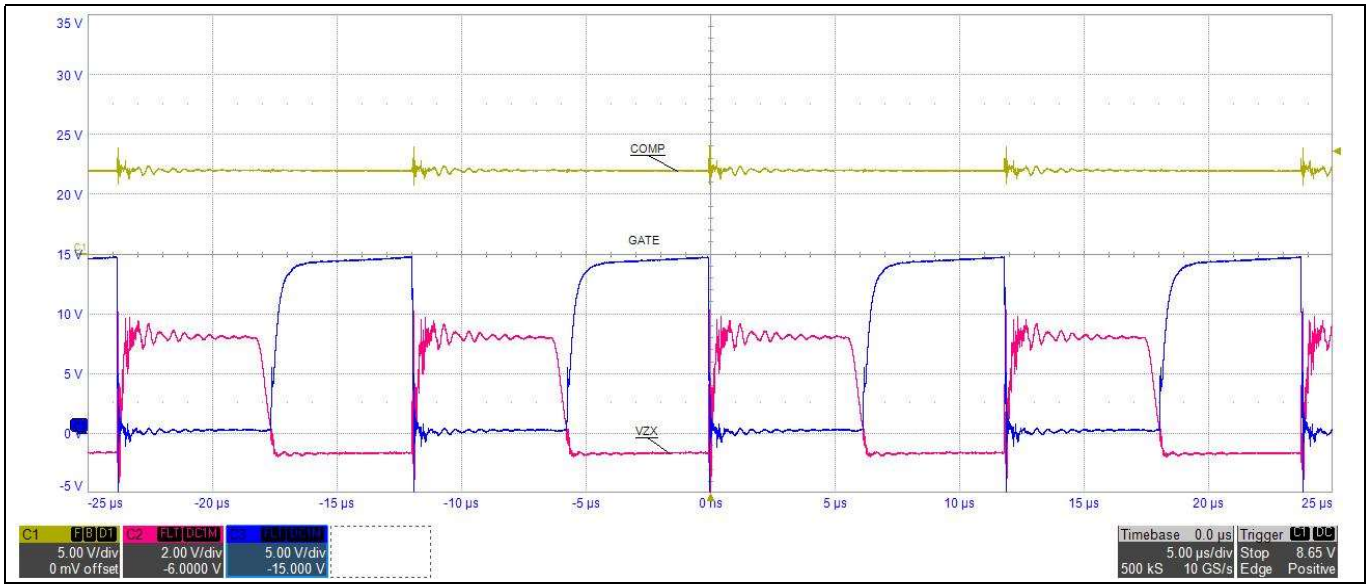


Figure 32 **120 V AC_{RMS} steady-state operation at 100 percent load: COMP voltage (yellow), Primary MOSFET gate V_{GS} (blue), zero crossing voltage V_{ZX} (red)**

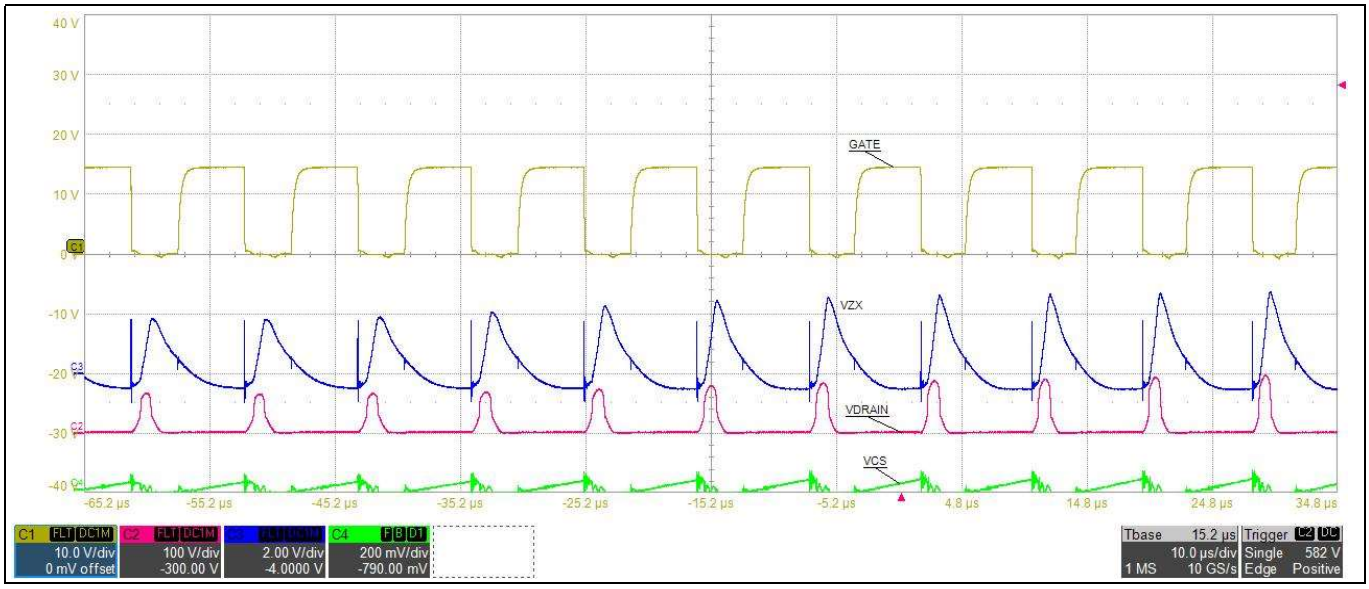


Figure 33 **120 V AC_{RMS} line zero crossing: MOSFET gate V_{GS} (yellow), zero crossing voltage V_{ZX} (blue), Primary MOSFET drain voltage (red), current sense voltage (V_{CS})**

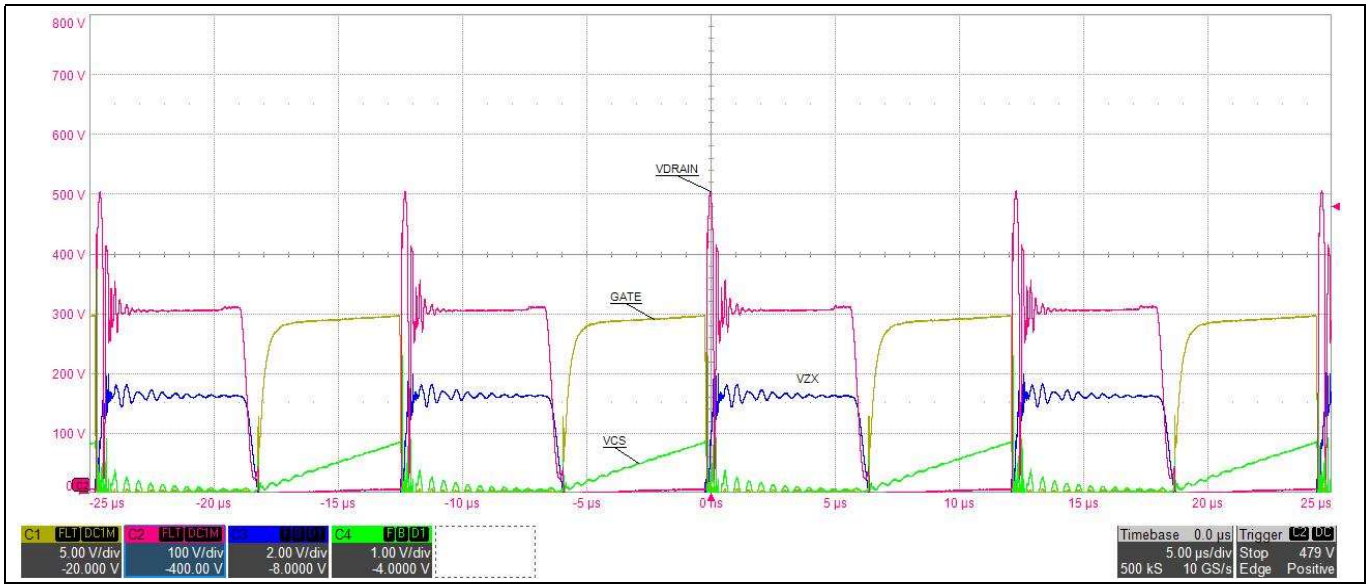


Figure 34 **120 V AC_{RMS} steady-state operation at 100 percent load: drain voltage V_{DS} (red), Primary MOSFET gate V_{GS} (yellow), current sense voltage V_{CS} (green), zero crossing voltage V_{ZX} (blue)**

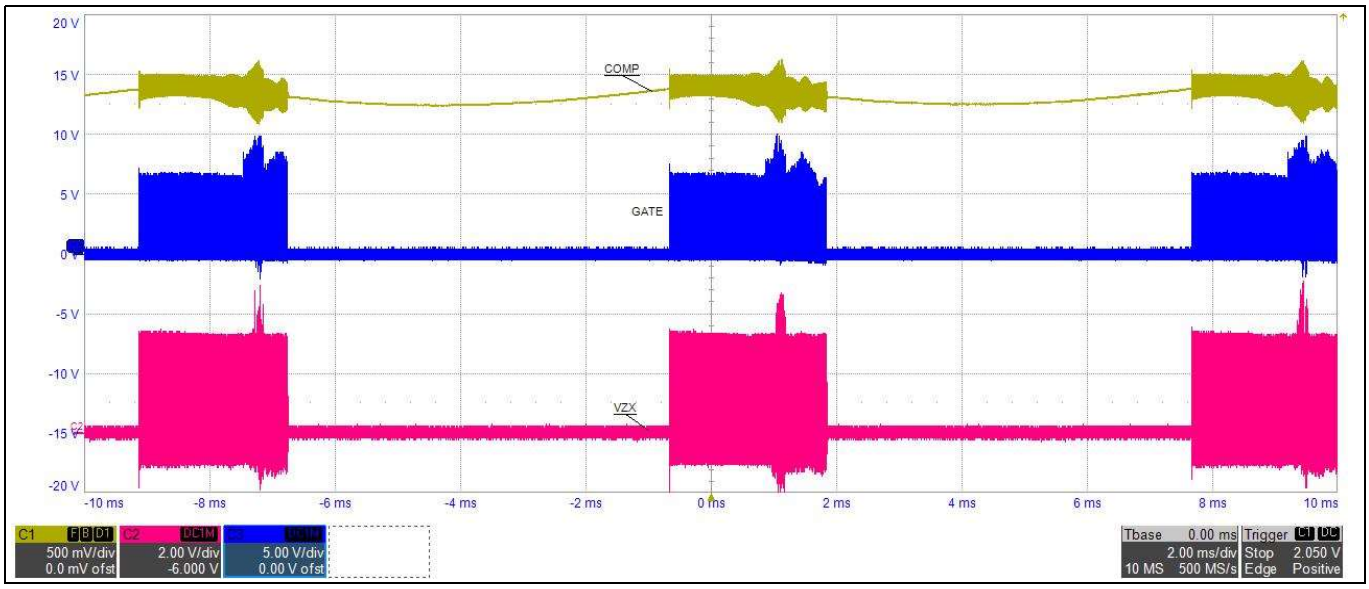


Figure 35 **No-load burst mode operation at 120 V AC_{RMS}: COMP voltage (yellow), Primary MOSFET gate voltage V_{GS} (blue), zero crossing voltage V_{zx} (red)**

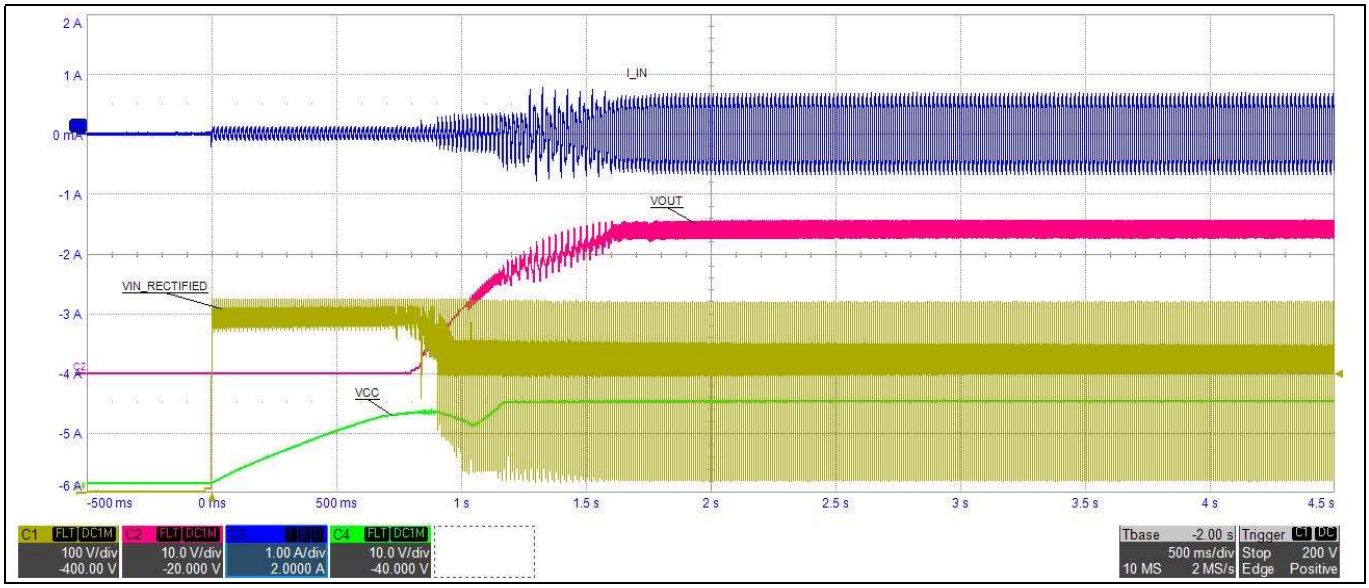


Figure 36 **230 V AC_{RMS} start-up operation at 100 percent load: output voltage V_{OUT} (red), input current (blue), rectified input voltage (yellow), V_{CC} (green)**

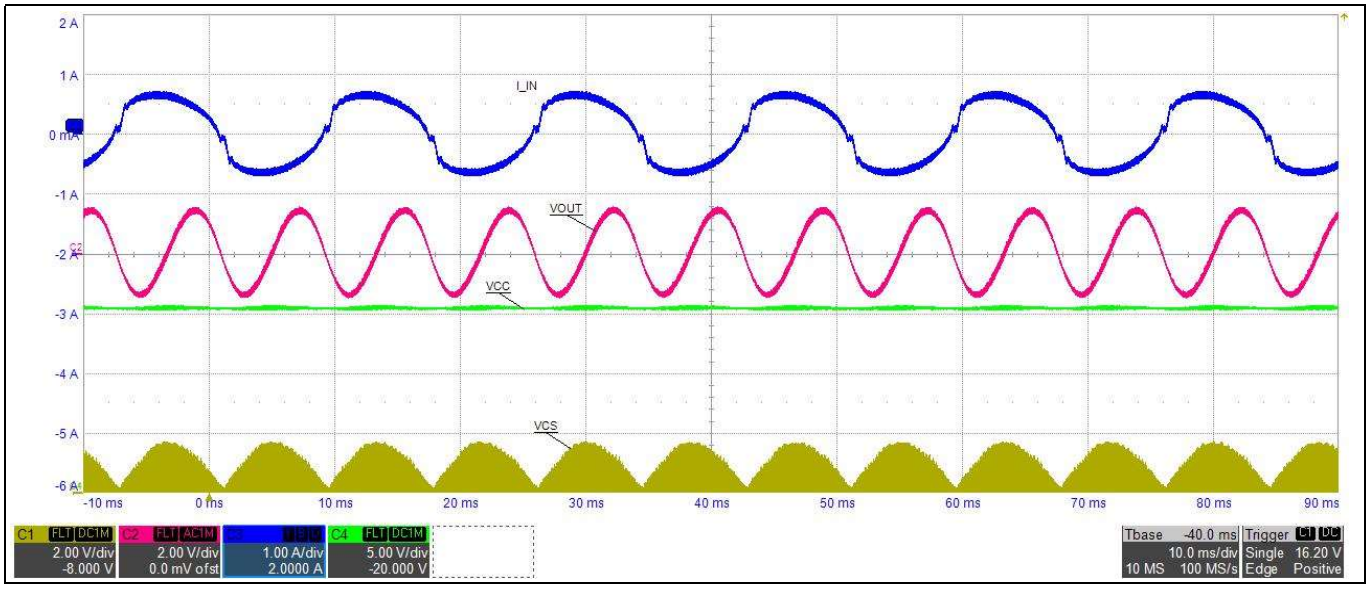


Figure 37 **230 V AC_{RMS} steady-state operation at 100 percent load: output voltage V_{OUT} ripple (red), input current (blue), current sense V_{CS} (yellow), V_{CC} (green)**

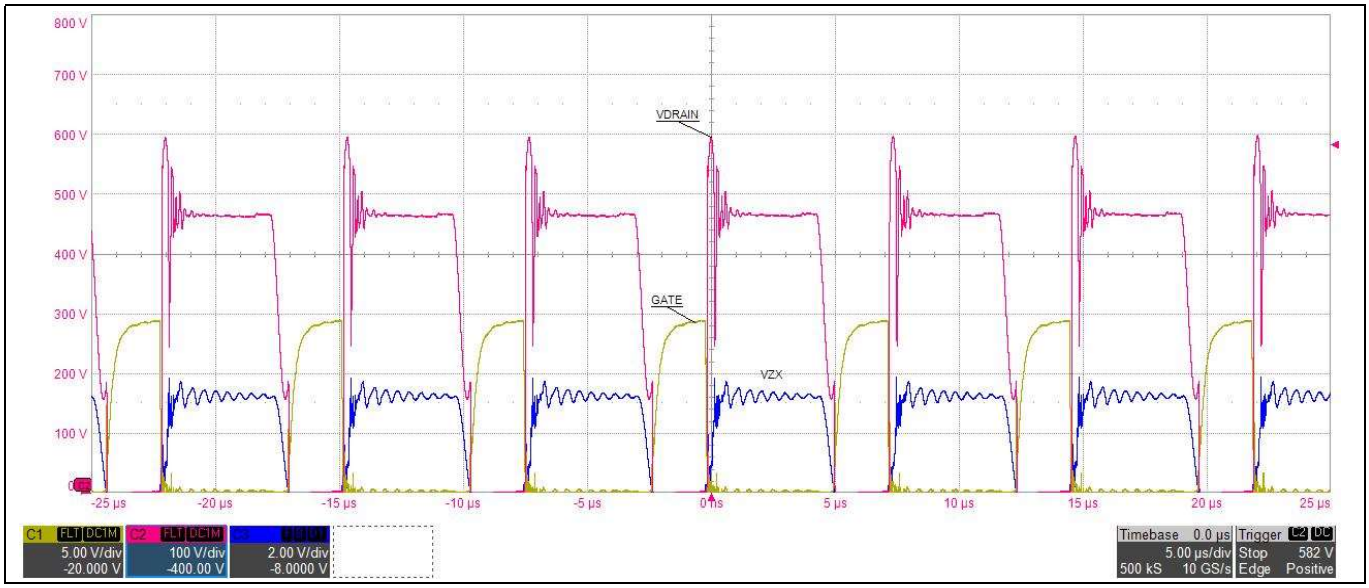


Figure 38 **230 V AC_{RMS} steady-state operation at 100 percent load: drain voltage V_{DS} (red), Primary MOSFET gate V_{GS} (yellow), current sense voltage V_{CS} (green), zero crossing voltage V_{ZX} (blue)**

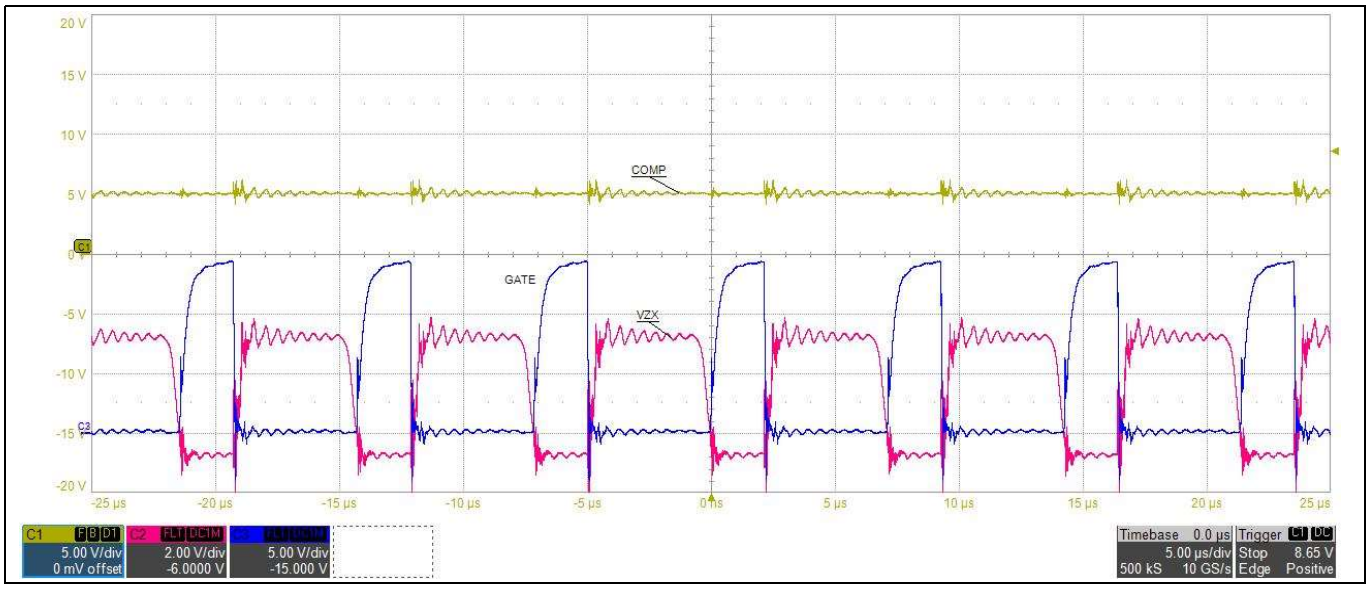


Figure 39 **230 V AC_{RMS} steady-state operation at 100 percent load: COMP voltage (yellow), Primary MOSFET gate V_{GS} (blue), zero crossing voltage V_{ZX} (red)**

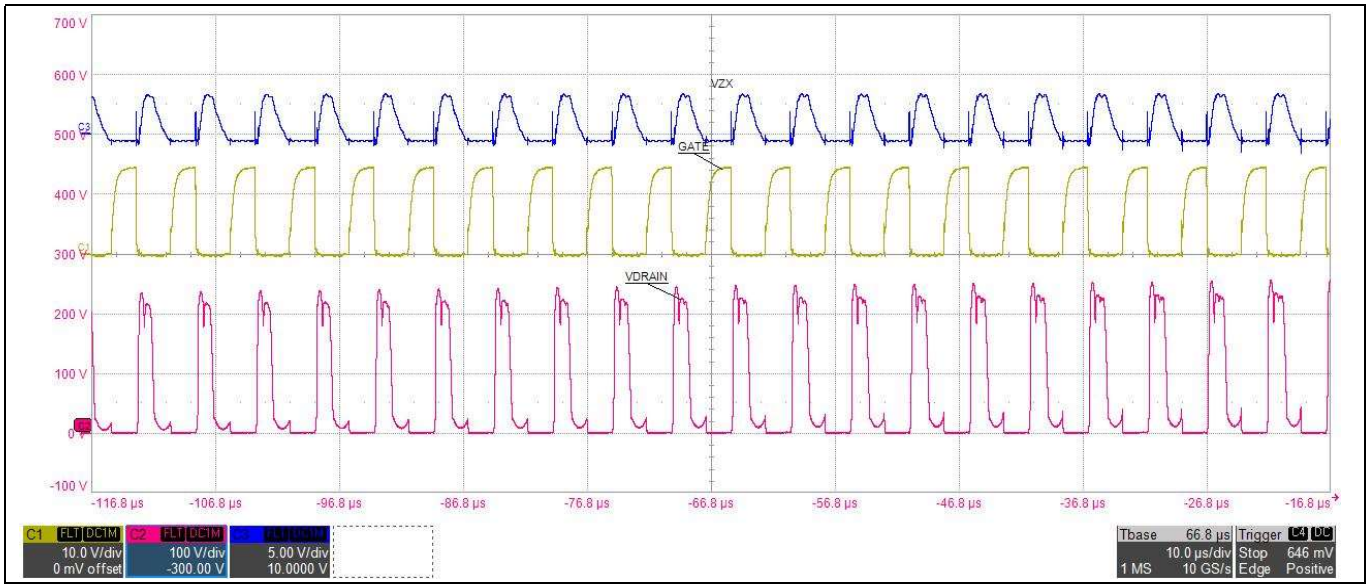


Figure 40 **230 V AC_{RMS} line zero crossing: MOSFET gate V_{GS} (yellow), zero crossing voltage V_{ZX} (blue), Primary MOSFET drain voltage (red)**

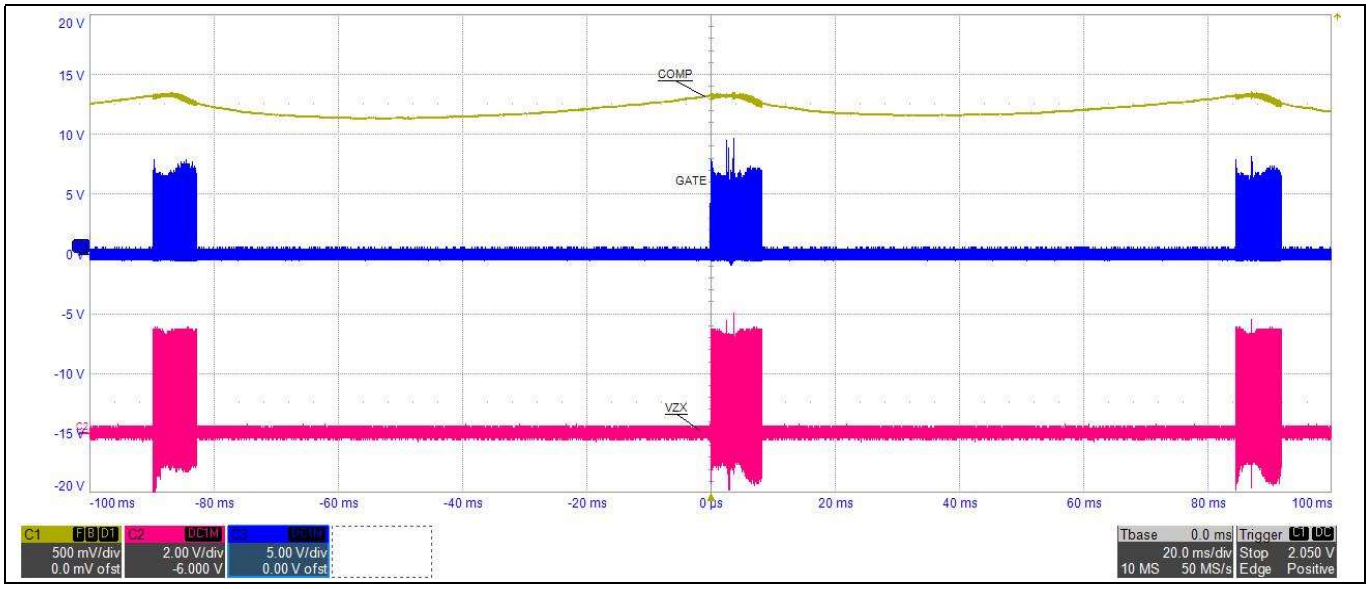


Figure 41 **No-load burst mode operation at 230 V AC_{RMS}: COMP voltage (yellow), Primary MOSFET gate voltage V_{GS} (blue), zero crossing voltage V_{zx} (red)**

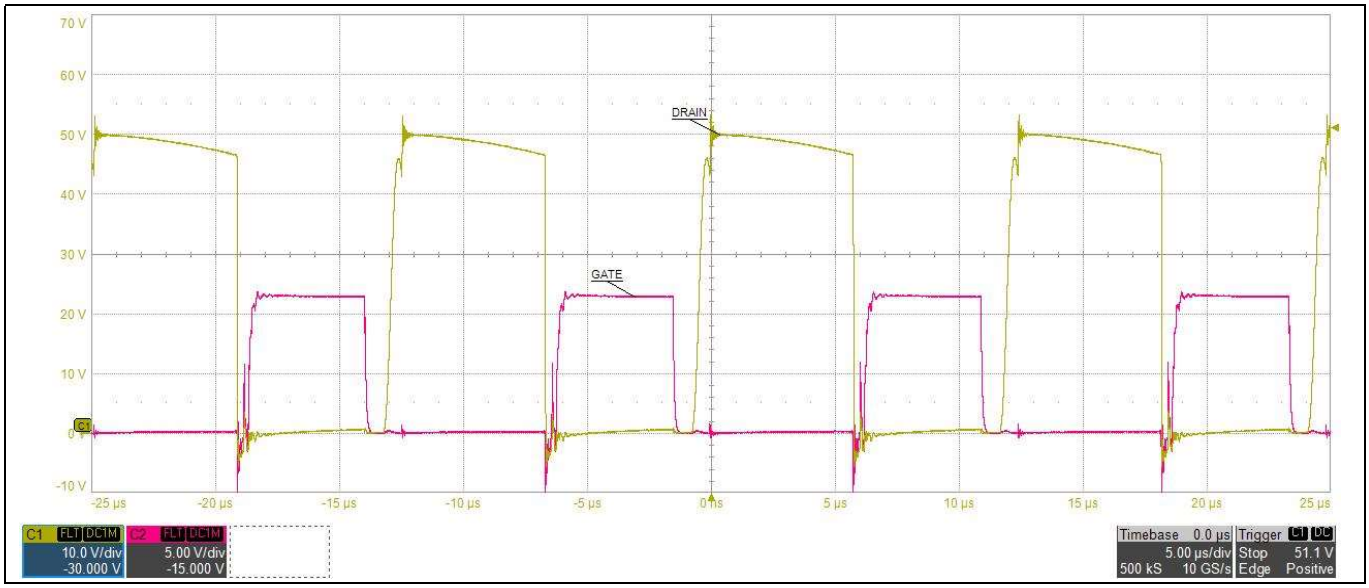


Figure 42 **120 V AC_{RMS} steady-state operation at 100 percent load: Secondary MOSFET drain voltage V_{DS} (yellow), MOSFET V_{GS} (red)**

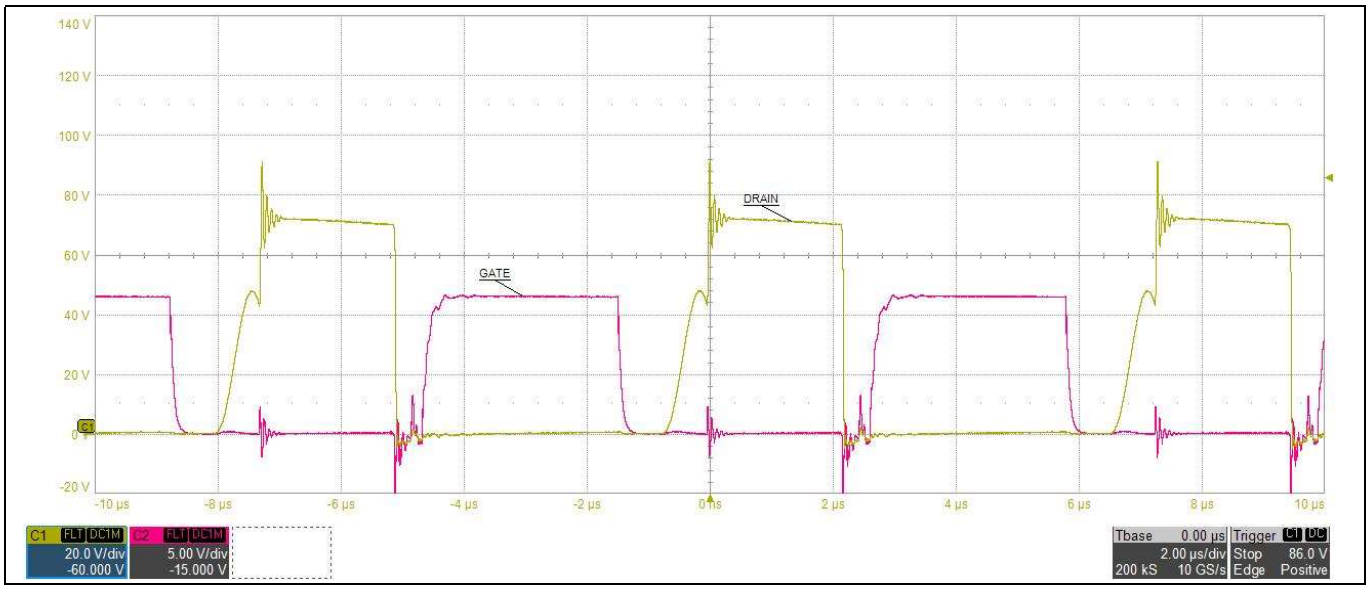


Figure 43 **230 V AC_{RMS} steady-state operation at 100 percent load: Secondary MOSFET drain voltage V_{DS} (yellow), MOSFET V_{GS} (red)**

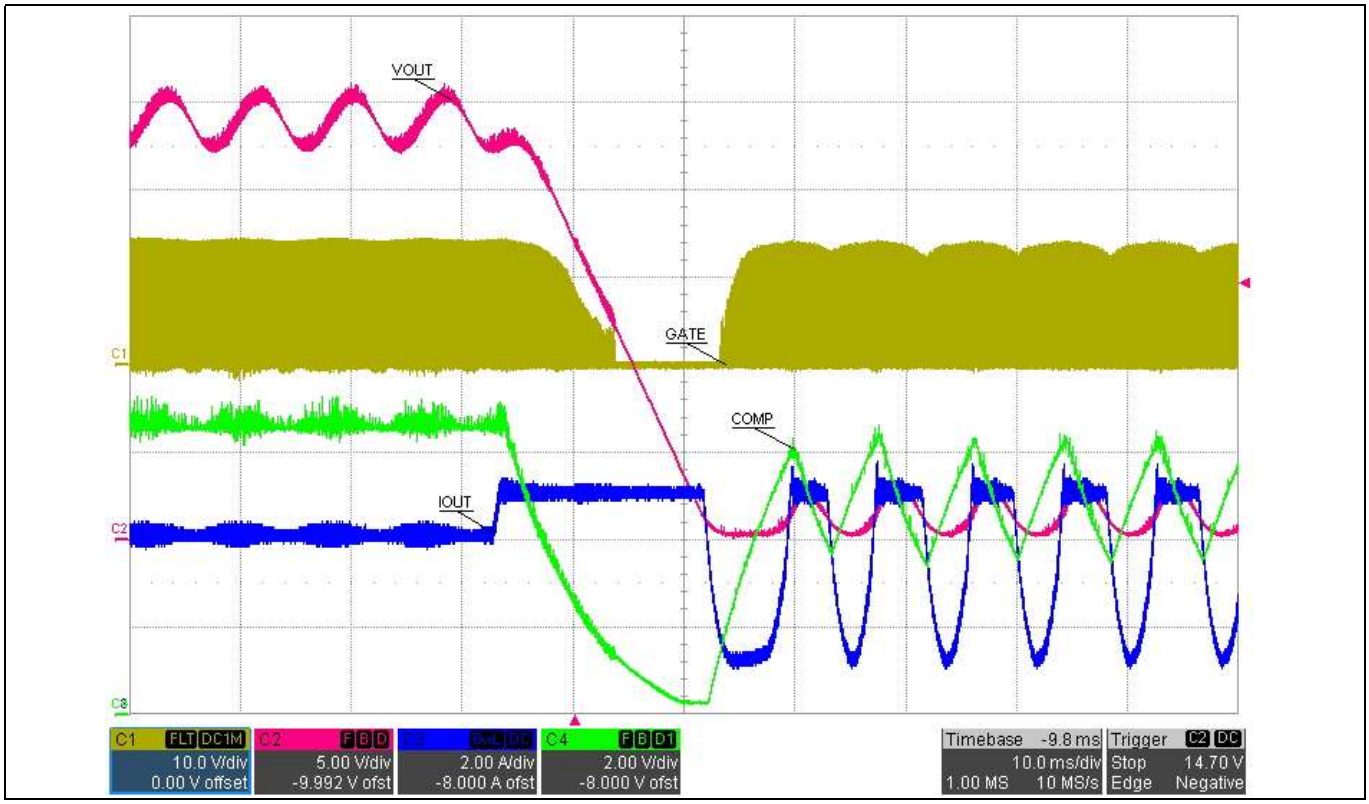


Figure 44 Overload from 4.2 A to 5 A
Primary MOSFET V_{GS} (yellow), V_{OUT} (red), I_{OUT} (blue), COMP (green)

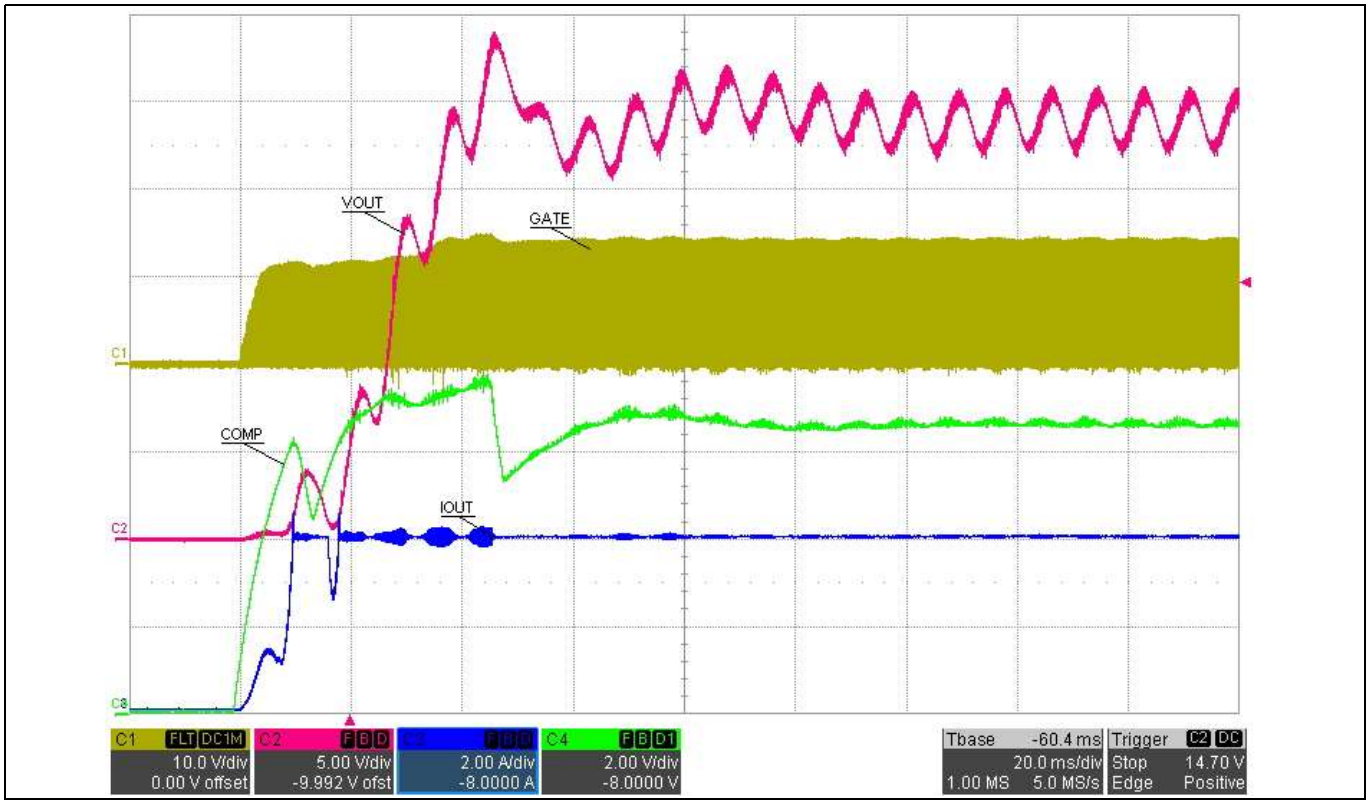


Figure 45 Overload recovery from 5 A to 4.2 A
Primary MOSFET V_{GS} (yellow), V_{OUT} (red), I_{OUT} (blue), COMP (green)

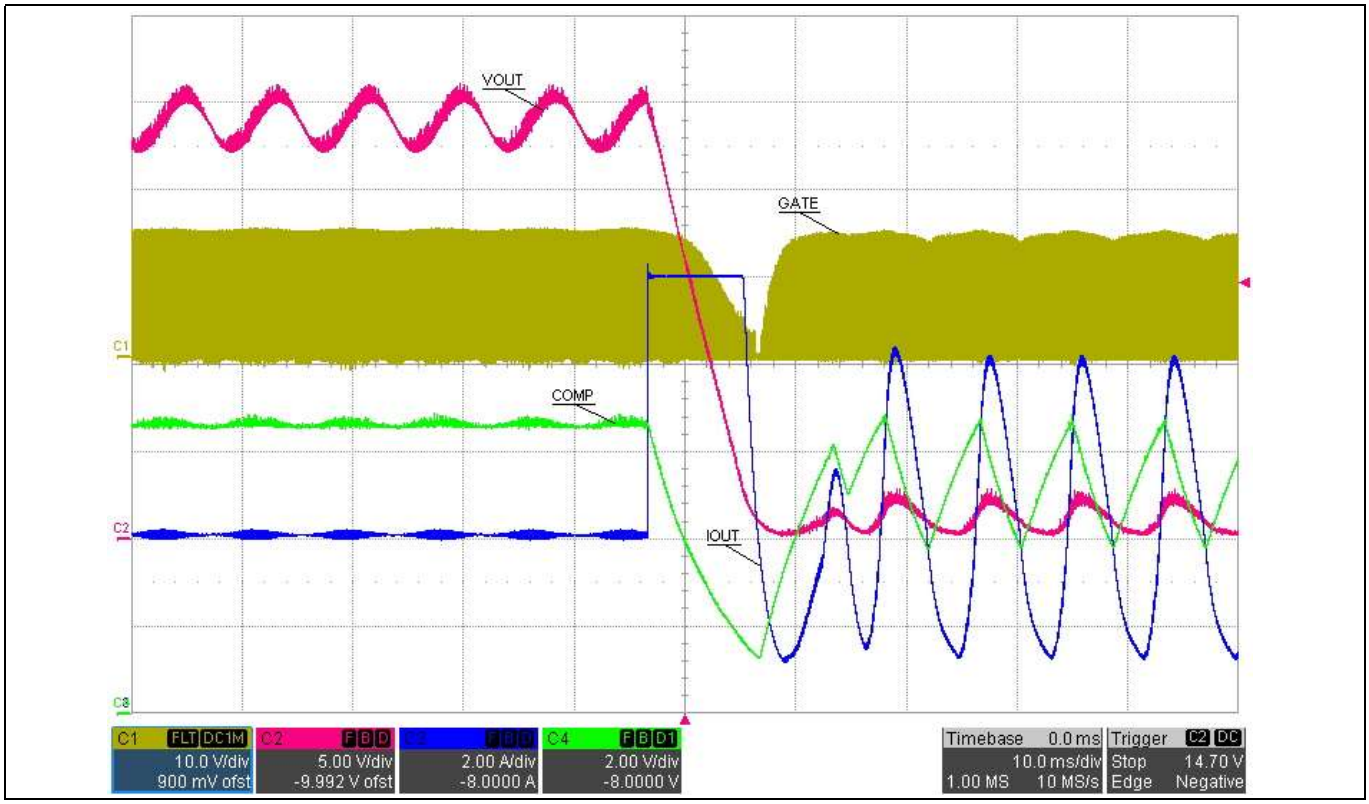


Figure 46 **Output short circuit at 4.2 A**
Primary MOSFET V_{GS} (yellow), V_{OUT} (red), I_{OUT} (blue), COMP (green)

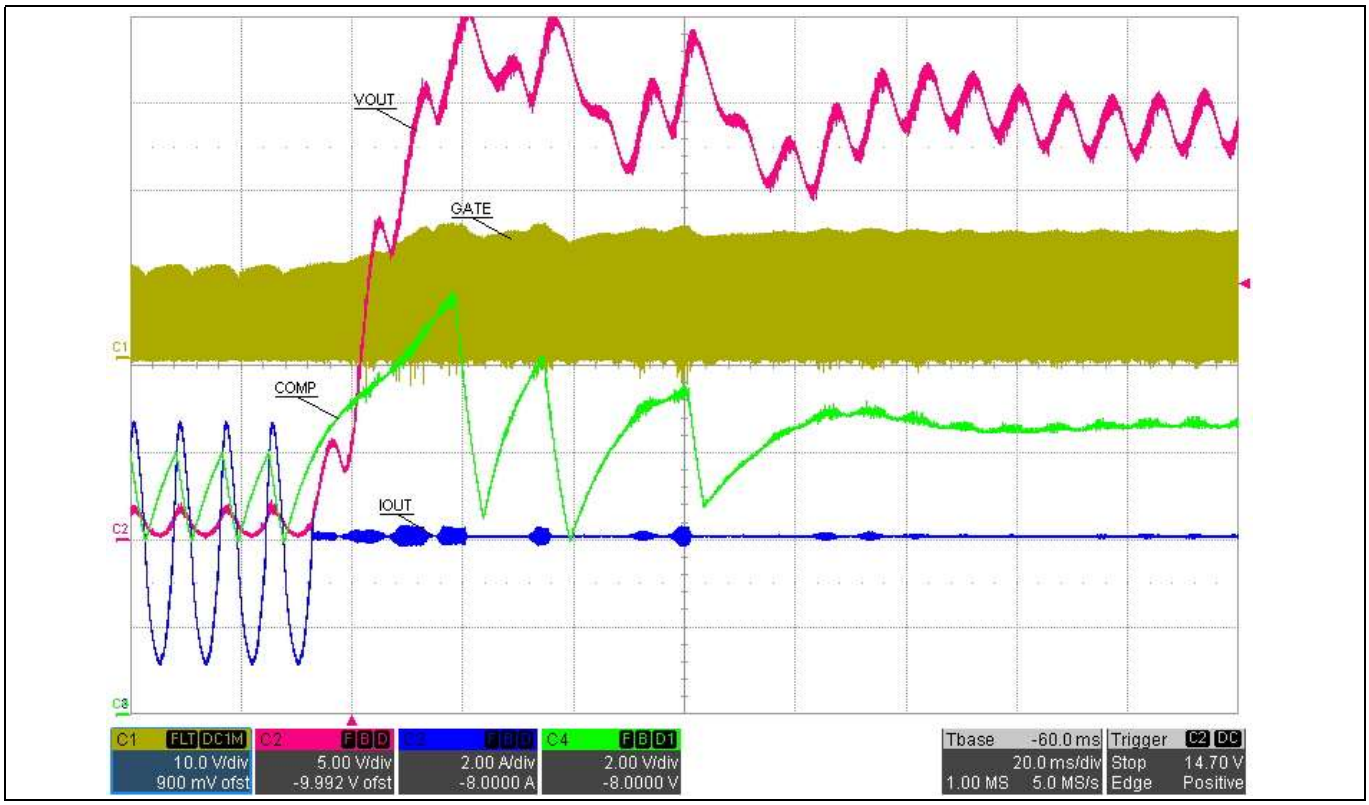


Figure 47 **Output short circuit recovery to 4.2 A**
Primary MOSFET V_{GS} (yellow), V_{OUT} (red), I_{OUT} (blue), COMP (green)

12.2 Thermal performance under normal operating conditions

Thermal images captured under conditions of 120 V AC input, 24 V/4.2 A load (after 1 hour of operation):

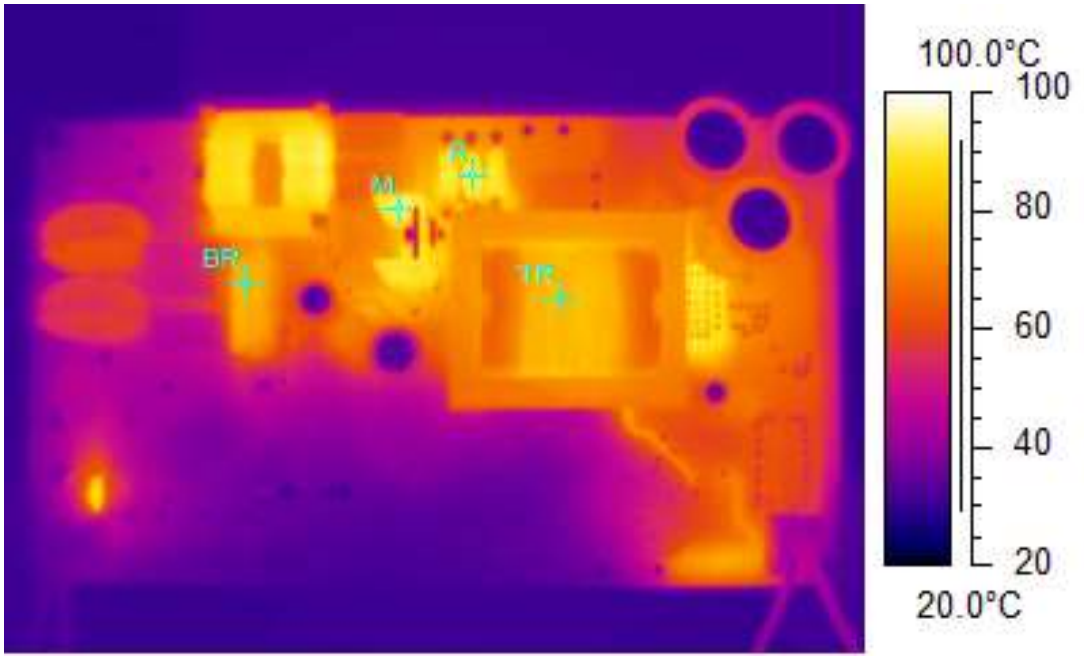


Figure 48 Top-side thermal image

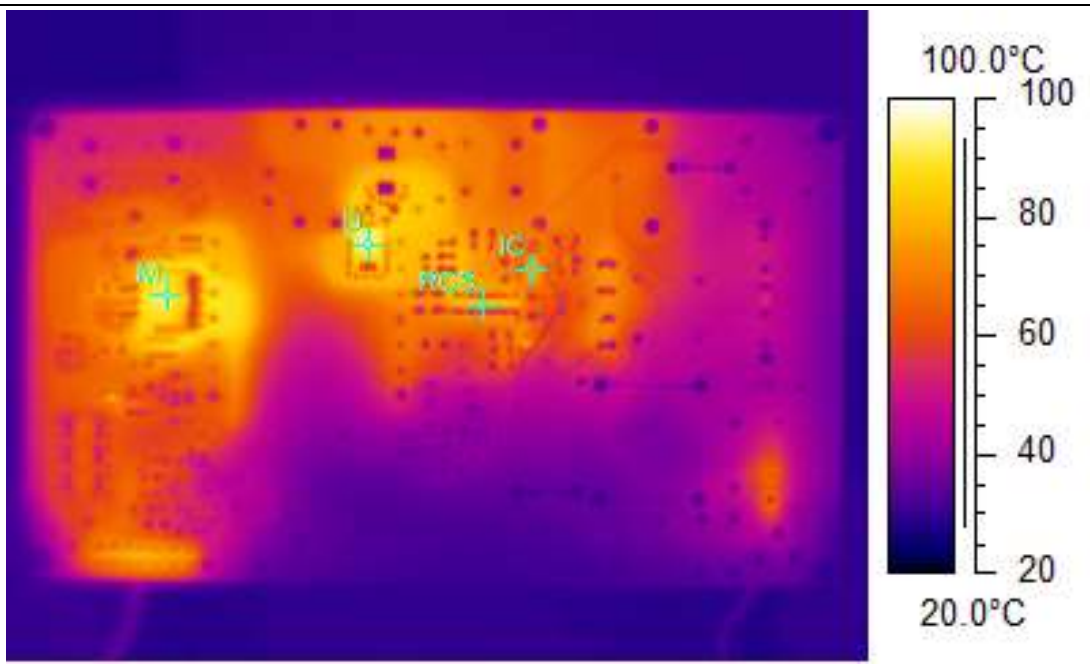
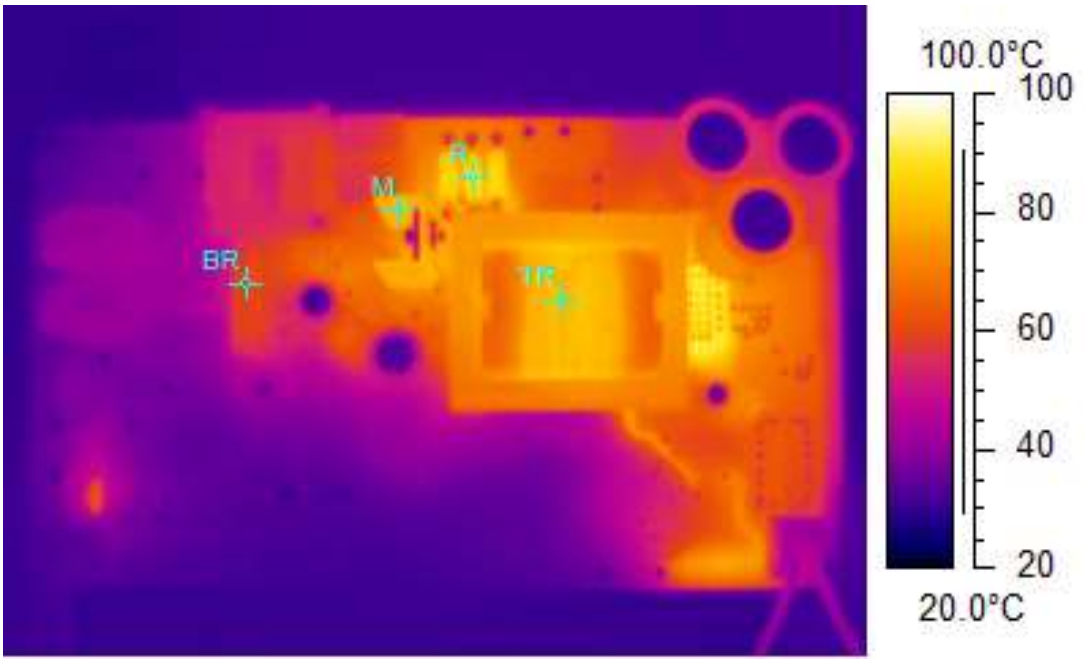


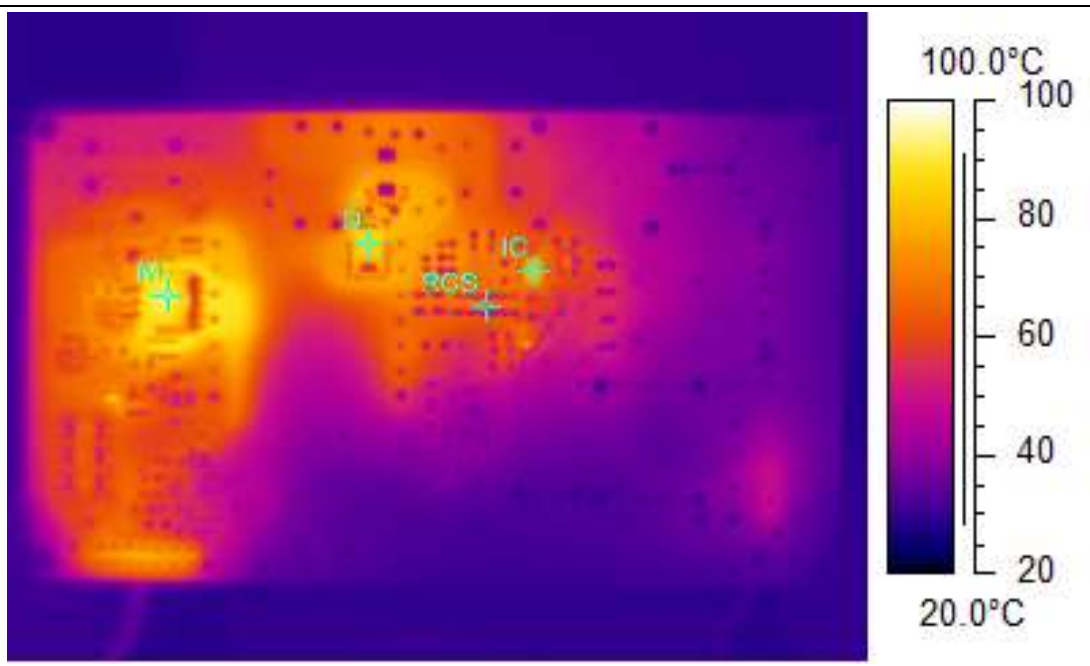
Figure 49 Bottom-side thermal image

Thermal images captured under conditions of 230 V AC_{RMS} input, 24 V/4.2 A load (after 1 hour of operation):



BR1	M2	R12	L1
59.8	81.2	87.0	80.8

Figure 50 Top-side thermal image



M1	D1	IC1	R23
91.7	87.8	67.6	84.1

Figure 51 Bottom-side thermal image

12.3 Conducted EMI

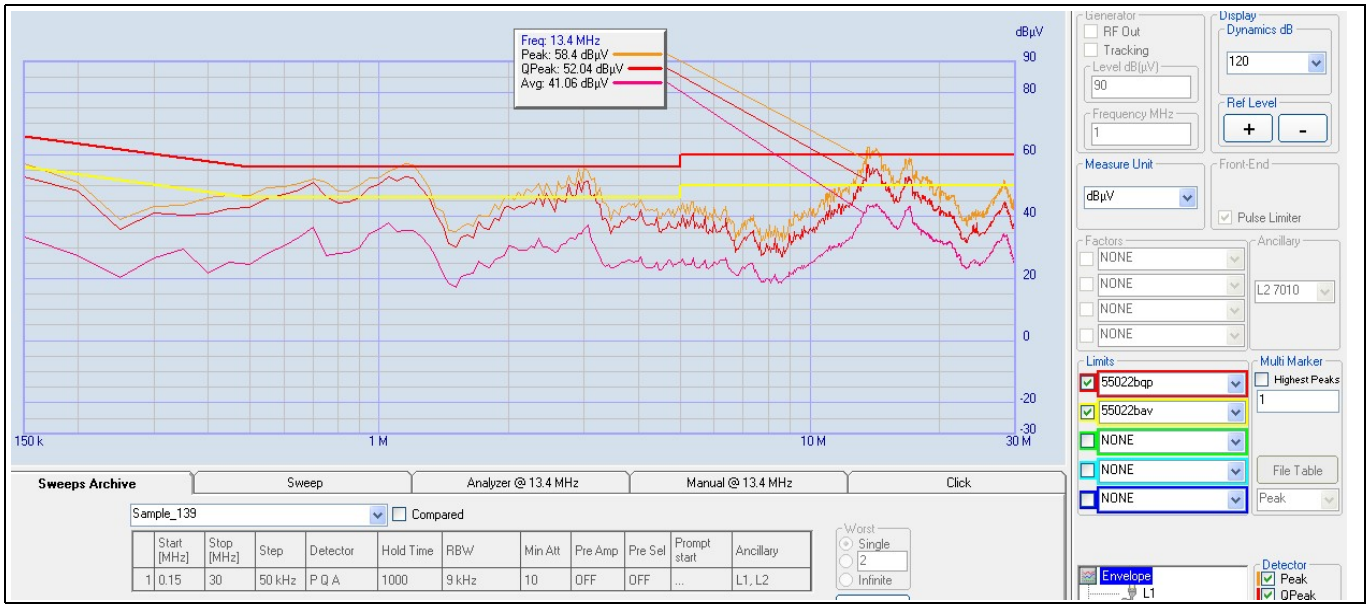


Figure 52 Conducted emissions at 120 V AC_{RMS} with 100 percent load

Figure 53 Conducted emissions at 230 V AC_{RMS} with 100 percent load

The limit lines in the above figures represent EN 55022 class B limits for the quasi-peak in red and average in yellow. Frequency sweep measurements are shown in red for quasi-peak and pink for average. The results provided here are from pre-compliance tests only. These were not carried out at a certified test lab. For compliance with the standard the traces must remain below their respective limit lines for both quasi-peak and average measurements, as shown in the table below.

Tests were carried out using a 4.2 A resistive load. EMI emissions are very dependent on the board layout; please refer to section 9.1.

Table 5 EN 55022 class B limits for conducted EMI

CISPR22 class B conducted EMI limits		
Frequency emission (MHz)	**Quasi-peak**	**Average**
0.15 to 0.50	66 to 56*	56 to 46*
0.50 to 5.00	56	46
5.00 to 30.0	60	50
FCC part 15 class B conducted EMI limits		
Frequency emission (MHz)	**Quasi-peak**	**Average**
0.15 to 0.50	66 to 56*	56 to 46*
0.50 to 5.00	56	46
5.00 to 30.0	60	50
*Decreases with logarithm of the frequency		

Note
Infineon Technologies does not guarantee compliance with any EMI standard.

13 Conclusion

The DEMO_100W_24VDC_FB evaluation board demonstrates a low-cost single-stage PFC Flyback power supply design successfully implemented with the IRS2982S.

It has been shown that the IRS2982S operating in CrCM is able to provide a very high power factor with low-line current THD over the input range. The benefits of SR using the IR1161L to improve efficiency and minimize output rectifier losses have also been demonstrated.

Furthermore operation over a wide line and load range can be achieved by moving to DCM operation at light loads using voltage mode control as long as rapid dynamic response is not required. The minimum off-time limit prevents the switching frequency from rising too high thereby limiting MOSFET switching losses. The secondary-side feedback circuit demonstrates a very tight voltage regulation over a wide load and line range. Accuracy of regulation over the output current range remains within +/-2.5 percent of the nominal output over the input line voltage range. It has been demonstrated that to achieve these results the control loop must be designed carefully to accommodate a wide line-load range while also maintaining stability and best possible power factor and iTHD.

The short-circuit and over-load protection functions are implemented. Brown out protection has also been implemented with minimal external components. Both of these functions have been verified.

The start-up time of the power supply over the input voltage range is less than 2 s measured at 120 V AC_{RMS} and 230 V AC_{RMS} line inputs. The component temperatures on the board remain less than 85°C under all line and load conditions.

Test results show that the design specifications have been met.

References

[1] IRS2505LPBF SMPS control IC datasheet, Infineon Technologies

[2] IRS2982S SMPS control IC datasheet, Infineon Technologies

[3] IRS2505L µPFC control IC design guide, Peter B. Green and Helen Ding, Infineon Technologies

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Revision history

Document version	Date of release	Description of changes
1.0	9/25/2019	First release
2.0	1/28/2020	Modified overload and short-circuit protection circuits. Test results updated. More test waveforms added. Minor corrections.

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